

# APW7236

## 1.5MHz Step-Up Converter for White LEDs

### Features

- Wide Input Voltage from 2.7V to 6V
- Fixed 1.5MHz Switching Frequency
- Reference Voltage : 0.2V
- PWM Brightness Control with Wide Frequency Range of 100Hz to 100kHz
- Build-In Power MOSFET : 0.2A
- Open-LED Protection
- Under-Voltage Lockout Protection
- Over-Temperature Protection
- $<1\mu\text{A}$  Quiescent Current during Shutdown
- TSOT-23-6A and TDFN2x2-8 Package
- Halogen and Lead Free Available (RoHS Compliant)

### Applications

- White LED Display Backlighting
- Cell Phone and Smart Phone
- PDA, PMP, MP3
- Digital Camera

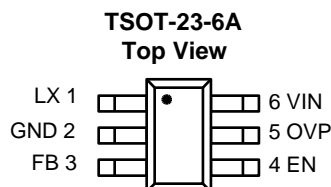
### General Description

The APW7236 is a current-mode and fixed frequency boost converter with an integrated N-FET to drive white LEDs.

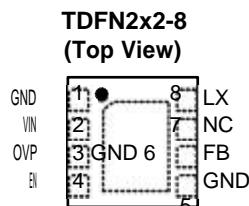
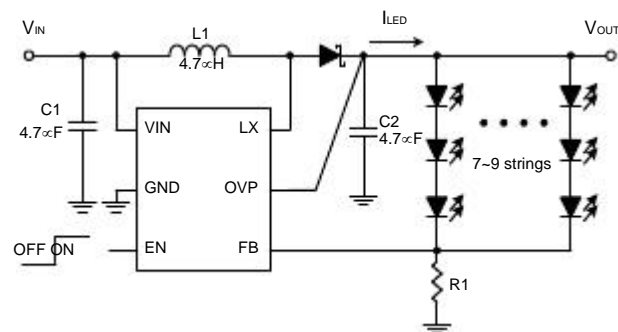
The series connection allows the LED current to be identical for uniform brightness. Its low on-resistance of NFET and low feedback voltage reduce power loss and achieve high efficiency. Fast switching frequency (1.5MHz typical) allows using small-size inductor and both of input and output capacitors. An over voltage protection function, which monitors the output voltage via OVP pin, stops switching of the IC if the OVP voltage exceeds the over voltage threshold. An internal soft-start circuit eliminates the inrush current during start-up.

The APW7236 also integrates under-voltage lockout, over-temperature protection, and current limit circuits to protect the IC in abnormal conditions. The APW7236 is available in a TSOT-23-6A and TDFN2x2-8 package.

### Pin Configuration



### Simplified Application Circuit



JIATAIMU reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

# APW7236

## Ordering and Marking Information

APW7236	Assembly Material Handling Code Temperature Range Package Code Over-Voltage Threshold Code	Over-Voltage Threshold Code A: 24V B: 16V Package Code CT : 6 Lead TSOT-23 QB: TDFN2x2-8 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7236CT: 36YX	Y - Over-Voltage Threshold Code X - Date Code	APW7236QB: 36Y Y - Over-Voltage Threshold Code X X - Date Code

Note: JIATAIMU lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. JIATAIMU lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. JIATAIMU defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

## Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V <sub>IN</sub>	VIN Supply Voltage (VIN to GND)	-0.3 ~ 7	V
	FB, EN to GND	-0.3 ~ V <sub>IN</sub>	V
V <sub>LX</sub>	LX to GND Voltage	-0.3 ~ 27.5	V
V <sub>OVP</sub>	OVP to GND	-0.3 ~ 27.5	V
P <sub>D</sub>	Power Dissipation	Internally Limit	W
T <sub>J</sub>	Maximum Junction Temperature	150	°C
T <sub>STG</sub>	Storage Temperature	-65 ~ 150	°C
T <sub>SDR</sub>	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

## Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ <sub>JA</sub>	Junction-to-Ambient Resistance in Free Air <sup>(Note 2)</sup> TSOT-23-6A TDFN2x2-6	220 165	°C/W
θ <sub>JC</sub>	Junction-to-Case Resistance TSOT-23-6A TDFN2x2-6	120 20	°C/W

Note 2: θ<sub>JA</sub> is measured with the component mounted on a high effective thermal conductivity test board in free air.

# APW7236

## Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V <sub>IN</sub>	VIN Supply Voltage (VIN to GND)	2.7 ~ 6	V
V <sub>OVP</sub>	VOOUT to GND	V <sub>IN</sub> ~ 22	V
C <sub>IN</sub>	Input Capacitor	4.7~	μF
C <sub>OUT</sub>	Output Capacitor	4.7 ~	μF
L1	Converter Output Inductor	2.2 ~ 10	μH
T <sub>A</sub>	Ambient Temperature	-40 ~ 85	°C
T <sub>J</sub>	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the application circuit.

## Electrical Characteristics

Refer to figure 1 in the “Typical Application Circuits”. These specifications apply over V<sub>IN</sub> = 3.6V, T<sub>A</sub> = 25°C.

Sym bol	Pa rameter	Test Conditions	APW7236			Unit	
			Min.	Typ.	Max.		
SUPPLY CURRENT							
V <sub>IN</sub>	Input Voltage Range		2.5	-	6	V	
I <sub>DD 1</sub>	Input DC Bias Current	V <sub>FB</sub> = 0.4V, no switching	-	300	-	∞A	
I <sub>DD 2</sub>		V <sub>FB</sub> = GND, switching	-	2	5	mA	
I <sub>SD</sub>		EN=GND	-	-	1	∞A	
UNDER-VOLTAGE LOCKOUT							
	UVLO Threshold Voltage	V <sub>IN</sub> Rising	2.0	2.2	2.4	V	
	UVLO Hysteresis Voltage	V <sub>IN</sub> Falling	50	100	150	mV	
REFERENCE AND OUTPUT VOLTAGE							
V <sub>REF</sub>	Regulated Feedback Voltage	APW7236A/B	V <sub>IN</sub> =2.7V~6V, T <sub>A</sub> = 25 C °	0.185	0.2	0.215	V
			V <sub>IN</sub> =2.7V~6V, T <sub>A</sub> = -40 ~ 85 C °	0.18	-	0.22	V
I <sub>FB</sub>	FB Input Current		-50	-	50	nA	
INTERNAL POWER SWITCH AND SCHOTTKY DIODE							
F <sub>SW</sub>	Switching Frequency		1.25	1.5	1.75	MHz	
R <sub>ON</sub>	Power Switch On Resistance		-	0.2	-	&	
I <sub>LIM</sub>	Power Switch Current Limit		-	2	-	A	
	LX Leakage Curr ent	V <sub>EN</sub> = 0V, V <sub>LX</sub> = 0V or 6V, V <sub>IN</sub> = 6V	-1	-	1	∞A	
D <sub>MAX</sub>	LX Maximum Duty Cycle		92	95	98	%	

# APW7236

## Electrical Characteristics (Cont.)

Refer to figure 1 in the “Typical Application Circuits”. These specifications apply over  $V_{IN} = 3.6V$ ,  $T_A = 25^{\circ}C$ .

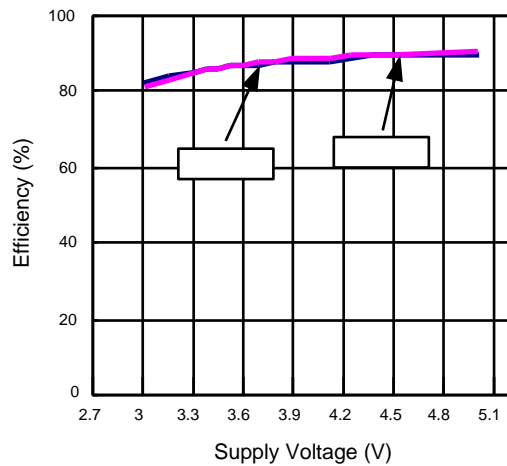
Symbol	Parameter	Test Conditions		APW7236			Unit
				Min.	Typ.	Max.	
OUTPUT OVER-VOLTAGE PROTECTION							
	Over Voltage Threshold	V <sub>OUT</sub> Rising	APW7236A	22	24	27.5	V
			APW7236B	14.5	16	20	V
	Over Voltage Hysteresis	V <sub>OVP</sub> Falling	-	3	-	V	
	OVP Leakage	V <sub>OVP</sub> =20V	-	50	-	αA	
ENABLE AND SHUTDOWN							
	Enable Voltage Threshold	V <sub>EN</sub> Rising	1	-	-	V	
	Shutdown Voltage Threshold	V <sub>EN</sub> Falling	-	-	0.4	V	
	EN Leakage Current	V <sub>EN</sub> = 0 ~ 6V, V <sub>IN</sub> = 6V	-2	-	2	αA	
	EN Minimum On Pluse Width	V <sub>EN</sub> = 0 ~ 6V, V <sub>IN</sub> = 6V, PWM Dimming Frequency=100Hz to 100kHz	-	800	-	ns	
OVER-TEMPERATURE PROTECTION							
T <sub>OTP</sub>	Over-Temperature Protection (Note 4)	T <sub>J</sub> Rising	-	150	-	°C	
	Over-Temperature Protection Hysteresis (Note 4)	T <sub>J</sub> Falling	-	40	-	°C	

Note 4: Guaranteed by design, not production tested.

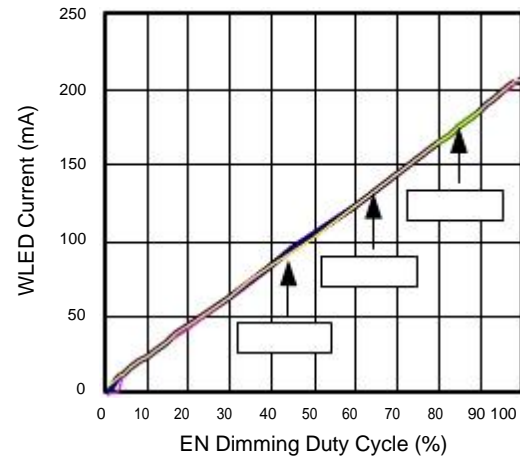
## Typical Operating Characteristics

(Refer to the application circuit in the section "Typical Application Circuits",  $V_{IN}=3.6V$ ,  $T_A=25^{\circ}C$ , 6WLEDs unless otherwise specified )

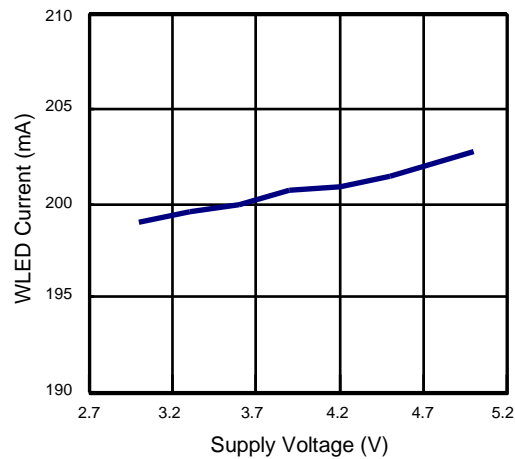
**Supply Voltage vs. Efficiency**



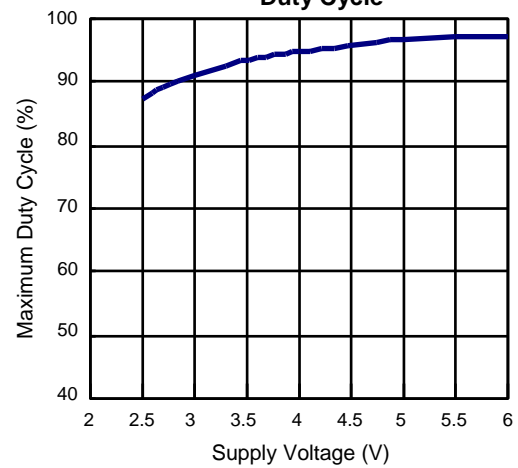
**EN Dimming Duty Cycle vs. WLED Current**



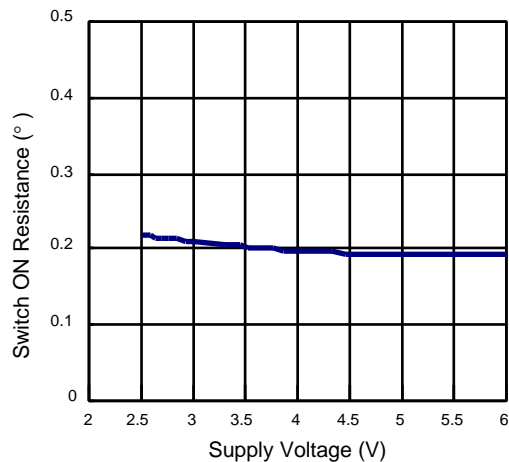
**Supply Voltage vs. WLED Current**



**Supply Voltage vs. Maximum Duty Cycle**



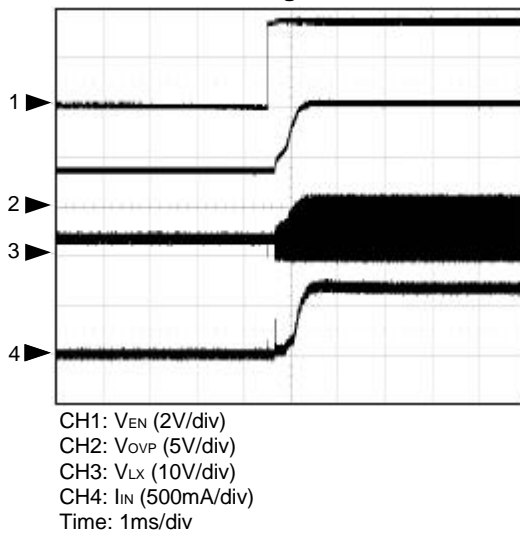
**Supply Voltage vs. Switch ON Resistance**



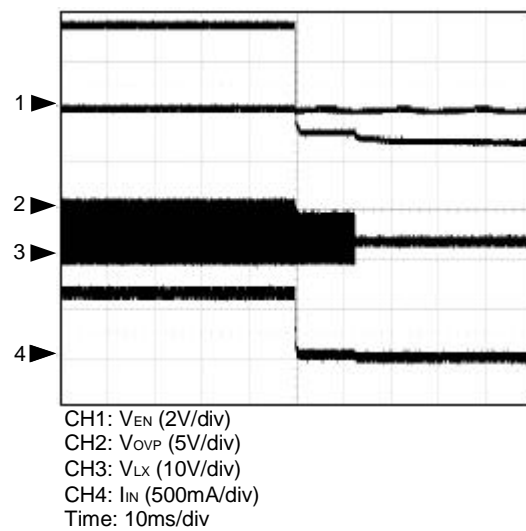
## Operating Waveforms

(Refer to the application circuit in the section "Typical Application Circuits",  $V_{IN}=3.6V$ ,  $T_A=25^{\circ}C$ , 6WLEDs unless otherwise specified )

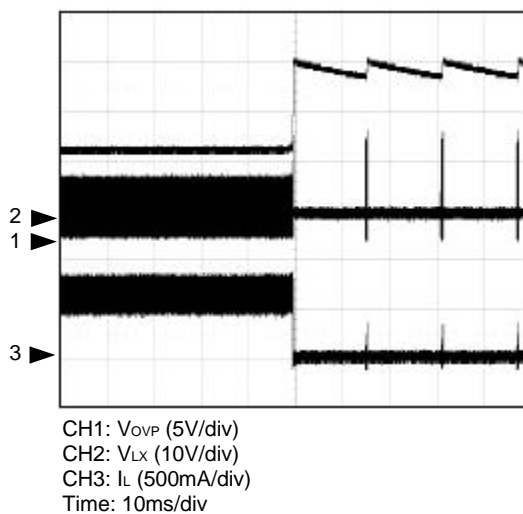
**EN Goes High- Enable**



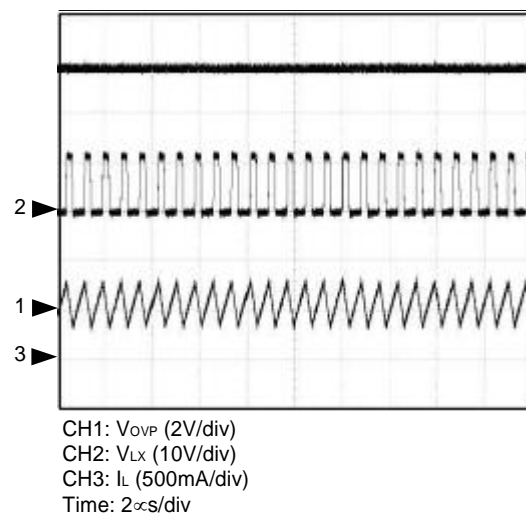
**EN Goes Low- Shutdown**



**OPEN-LED Protection**



**Normal Operation**

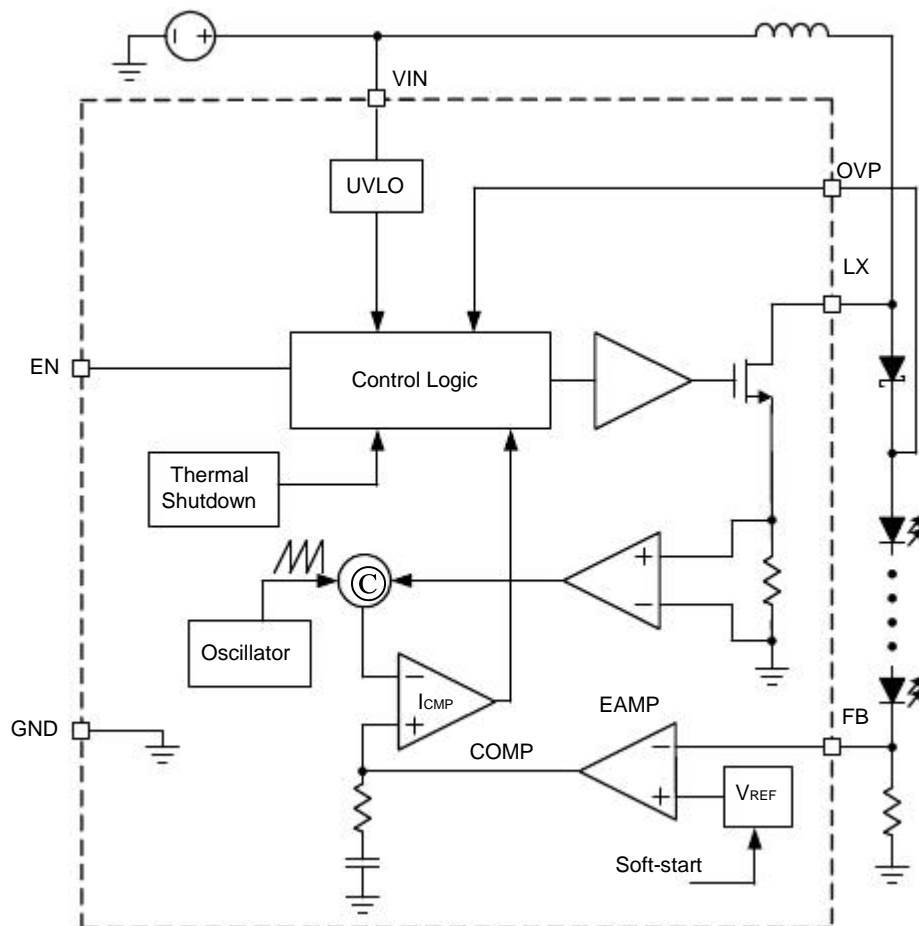


# APW7236

## Pin Description

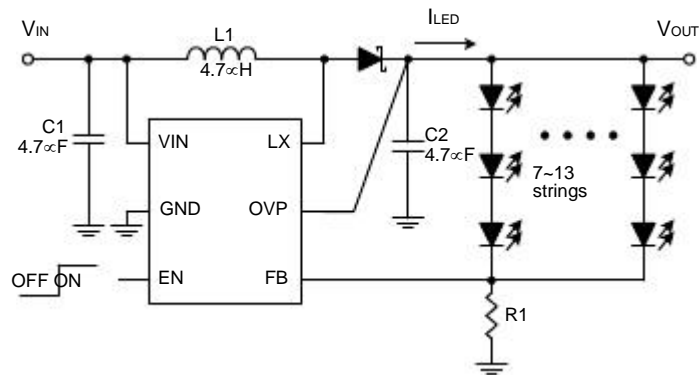
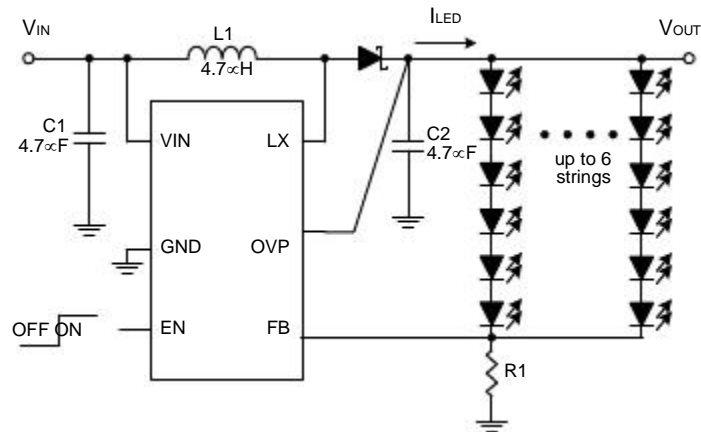
PIN			FUNCTION
NO.		NAME	
TDFN2x2-8	TSOT-23-6A		
1, 5	2	GND	Power and signal ground pin.
2	6	VIN	Main Supply Pin. Must be closely decoupled to GND with a 4.7 $\mu$ F or greater ceramic capacitor.
3	5	OVP	Converter Output and Over-Voltage Protection Input Pin.
4	4	EN	Enable Control Input. Forcing this pin above 1.0V enables the device, or forcing this pin below 0.4V to shut it down. In shutdown, all functions are disabled to decrease the supply current below 1 $\mu$ A. <b>Do not leave this pin floating.</b>
6	3	FB	Feedback Pin. Connect this pin to cathode of the lowest LED and current-sense resistor (R1). Calculate resistor value according to $R1=V_{REF}/I_{LED}$ .
7	-	NC	No Internal Connection.
8	1	LX	Switch pin. Connect this pin to inductor/diode here.
Exposed Pad	-	GND	Connecting this pad to GND.

## Block Diagram



# APW7236

## Typical Application Circuit



## Function Description

### Main Control Loop

The APW7236 is a constant frequency current-mode switching regulator. During normal operation, the internal N-channel power MOSFET is turned on each cycle when the oscillator sets an internal RS latch and turned off when an internal comparator (ICMP) resets the latch. The peak inductor current at which ICMP resets the RS latch is controlled by the voltage on the COMP node, which is the output of the error amplifier (EAMP). An external current-sense resistor connected between cathode of the lowest LED and ground allows the EAMP to receive a current feedback voltage  $V_{FB}$  at FB pin. When the LEDs voltage decreases to cause the LEDs current to decrease, it causes a slightly decrease in  $V_{FB}$  relative to the reference voltage, which in turn causes the COMP voltage to increase until the LEDs current reaches the set point.

### VIN Under-Voltage Lockout (UVLO)

The Under-Voltage Lockout (UVLO) circuit compares the input voltage at VIN with the UVLO threshold (2.2V rising, typical) to ensure the input voltage is high enough for reliable operation. The 100mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, startup begins. When the input voltage falls below the UVLO falling threshold, the controller turns off the converter.

### Soft-Start

The APW7236 has a built-in soft-start to control the N channel MOSFET current raises during start-up. During soft-start, an internal ramp voltage connected to one of the inverting inputs of the current limit comparator. The inductor current limit is proportional to the voltage. When the threshold voltage of the internal soft-start comparator is reached, the full current limit is released.

### Current-Limit Protection

The APW7236 monitors the inductor current, flowing through the N-channel MOSFET, and limits the current peak at current-limit level to prevent loads and the device from damages in overload conditions.

### Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7236. When the junction temperature exceeds 150 °C, a thermal sensor turns off the power MOSFET, allowing the device to cool. The thermal sensor allows the converter to start a soft-start process and regulate the LEDs current again after the junction temperature cools by 40 °C. The OTP is designed with a 40 °C hysteresis to lower the average Junction Temperature ( $T_J$ ) during continuous thermal overload conditions, increasing the lifetime of the device.

### Enable/Shutdown

Driving EN to ground places the APW7236 in shutdown mode. When in shutdown, the internal power MOSFET turns off, all internal circuitry shuts down and the quiescent supply current reduces to 1 µA maximum. This pin also could be used as a digital input allowing brightness controlled by using a PWM signal with frequency from 100Hz to 100kHz. The 0% duty cycle of PWM signal corresponds to zero LEDs current and 100% corresponds to full one. Suggestion dimming duty range is from 8% to 100% at 100kHz dimming frequency.

### Open-LED Protection

In driving LED applications, the feedback voltage on FB pin falls down if one of the LEDs, in series, is failed. Meanwhile, the converter unceasingly boosts the output voltage like an open-loop operation. Therefore, an over-voltage protection monitoring the output voltage via OVP pin is integrated into the chip to prevent the LX and the output voltages from exceeding their maximum voltage ratings. Once the voltage on the OVP pin rises above the OVP threshold, the converter stops switching and prevents the output voltage from rising. The converter can work again when the OVP voltage falls below the falling of OVP voltage threshold.

## Application Information

### Input Capacitor Selection

The input capacitor ( $C_{IN}$ ) reduces the current peaks drawn from the input supply and reduces noise injection into the IC. The reflected ripple voltage will be smaller with larger  $C_{IN}$ . For reliable operation, it is recommended to select the capacitor voltage rating at least 1.2 times higher than the maximum input voltage. The capacitors should be placed close to the  $V_{IN}$  and GND.

### Inductor Selection

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Especially at high-switching frequencies the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. A reasonable starting point for setting ripple current,  $\Delta I_L$ , is 30% to 50% of the average inductor current. The recommended inductor value can be calculated as below:

$$L \geq \left( \frac{V_{IN}}{V_{OUT}} \right)^2 \cdot \frac{V_{OUT} \Delta V_{IN}}{F_{SW} \cdot I_{OUT(MAX)}} \cdot \frac{1}{\left( \frac{\Delta I_L}{I_{L(AVG)}} \right)}$$

where

$V_{IN}$  = input voltage

$V_{OUT}$  = output voltage

$F_{SW}$  = switching frequency in MHz

$I_{OUT}$  = maximum output current in amp.

$\eta$  = Efficiency

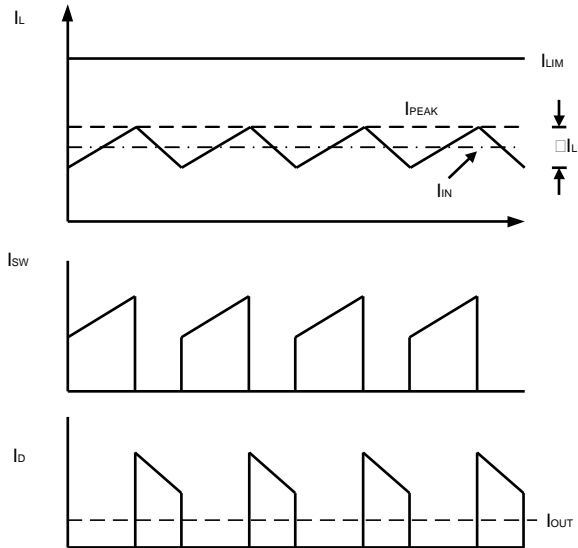
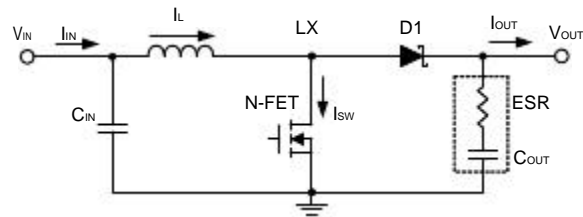
$\Delta I_L / I_{L(AVG)}$  = inductor ripple current/average current  
(0.3 to 0.5 typical)

To avoid saturation of the inductor, the inductor should be rated at least for the maximum input current of the converter plus the inductor ripple current. The maximum input current is calculated as below:

$$I_{IN(MAX)} = \frac{I_{OUT(MAX)} \cdot V_{OUT}}{V_{IN} \cdot \eta}$$

The peak inductor current is calculated as the following equation:

$$I_{PEAK} = I_{IN(MAX)} + \frac{1}{2} \frac{V_{IN} \ominus (V_{OUT} \ominus V_{IN})}{V_{IN}}$$



### Output Capacitor Selection

The current-mode control scheme of the APW7236 allows the usage of tiny ceramic capacitors. The higher capacitor value provides good load transient response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{COUT}$$

$$\Delta V_{ESR} \approx I_{PEAK} \cdot R_{ESR}$$

$$\Delta V_{COUT} \approx \frac{I_{PEAK}}{C_{OUT} \cdot f_{SW}}$$

where  $I_{PEAK}$  is the peak inductor current.

## Application Information (Cont.)

### Output Capacitor Selection (Cont.)

For ceramic capacitor application, the output voltage ripple is dominated by the  $\Delta V_{\text{COUT}}$ . When choosing the input and output ceramic capacitors, the X5R or X7R with their good temperature and voltage characteristics are recommended.

### Setting the LED Current

In figure 1, the converter regulates the voltage on FB pin, connected with the cathod of the lowest LED and the current-sense resistor R1, at 0.2V (typical). Therefore, the current ( $I_{\text{LED}}$ ), flowing via the LEDs and the R1, is calculated by the following equation:

$$I_{\text{LED}} = \frac{0.2 \text{ V}}{R1}$$

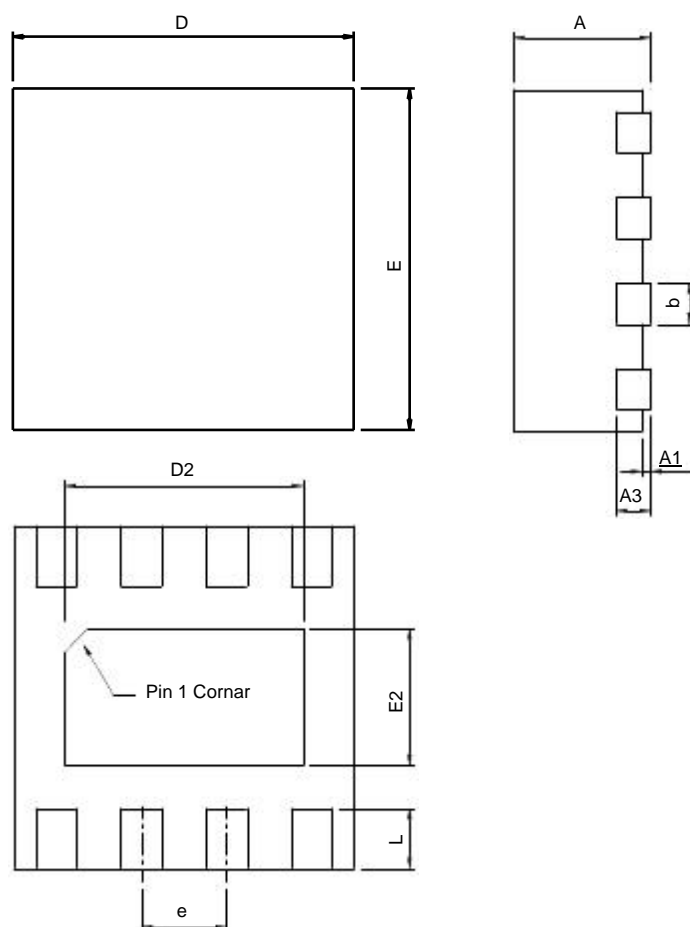
### Layout Considerations

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor should be placed close to the VIN and GND. Connecting the capacitor with VIN and GND pins by short and wide tracks without using any via holes for good filtering and minimizing the voltage ripple.
2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the LX pin to minimize the noise coupling into other circuits.
3. The feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.
4. A star ground connection or ground plane minimizes ground shifts and noise is recommended.

## Package Information

TDFN2x2-8



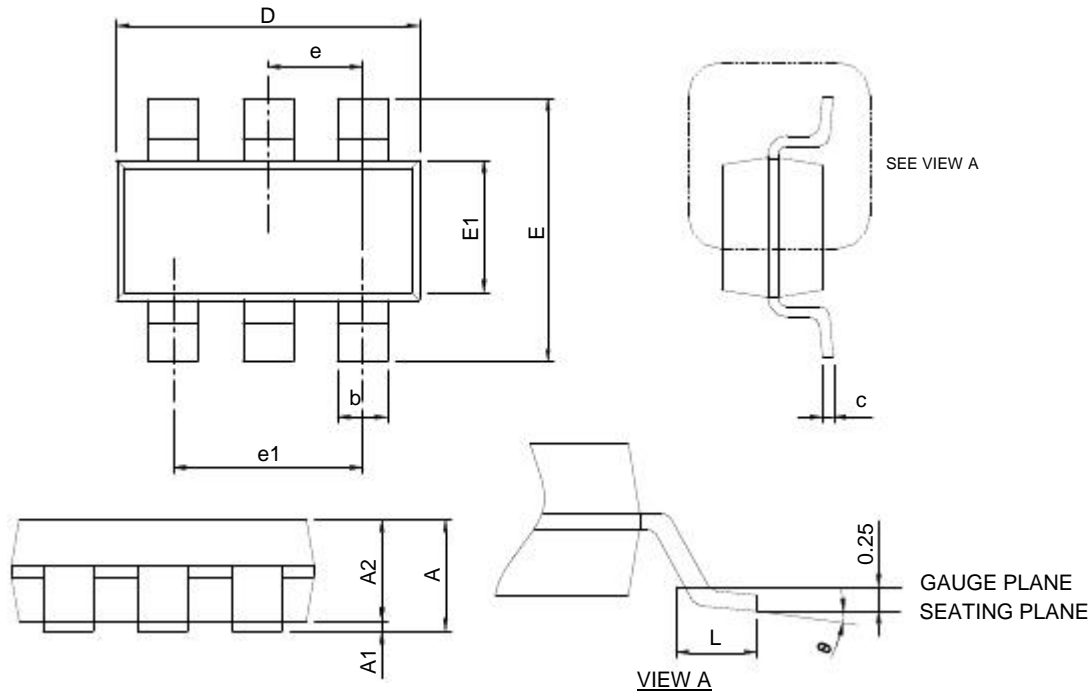
S Y M B O L	TDFN2x2-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	1.90	2.10	0.075	0.083
D2	1.00	1.60	0.039	0.063
E	1.90	2.10	0.075	0.083
E2	0.60	1.00	0.024	0.039
e	0.50 BSC		0.020 BSC	
L	0.30	0.45	0.012	0.018

Note : 1. Followed from JEDEC MO-229 WCCD-3.

# APW7236

## Package Information

TSOT-23-6A

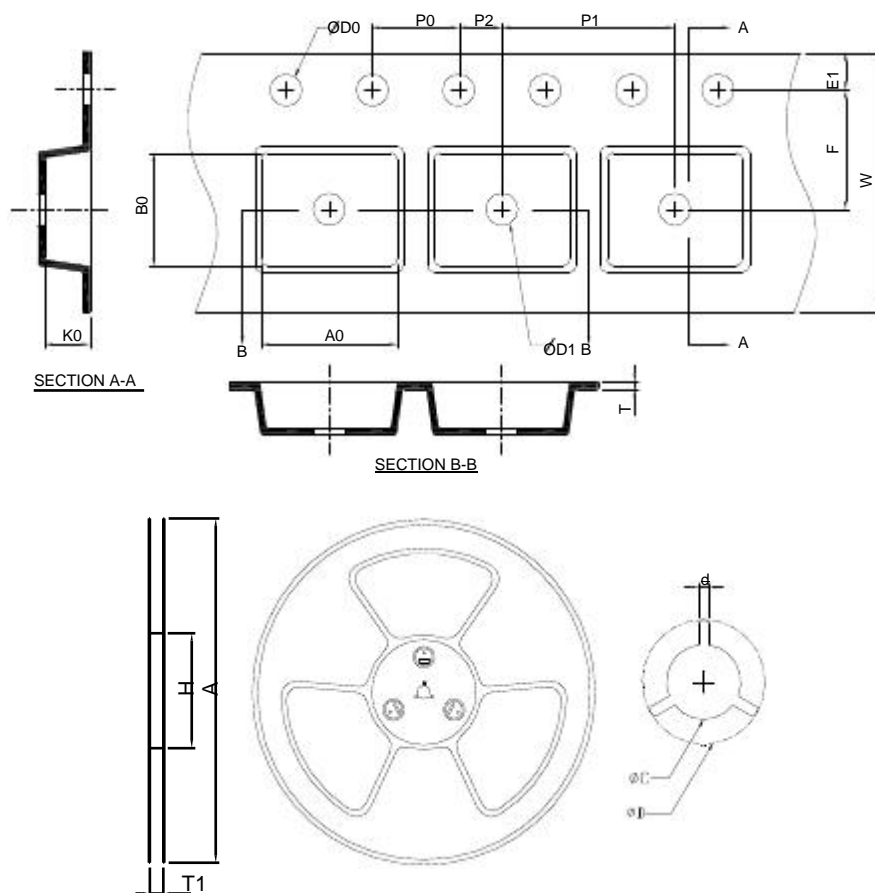


SYMBOL	TSOT-23-6A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	1.00	0.028	0.039
A1	0.01	0.10	0.000	0.004
A2	0.70	0.90	0.028	0.035
b	0.30	0.50	0.012	0.020
c	0.08	0.20	0.003	0.008
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

# APW7236

## Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN2x2-8	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.50±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.4	3.35 MIN	3.35 MIN	1.30±0.20
Application	A	H	T1	C	d	D	W	E1	F
TSOT-23-6A	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20

(mm)

# APW7236

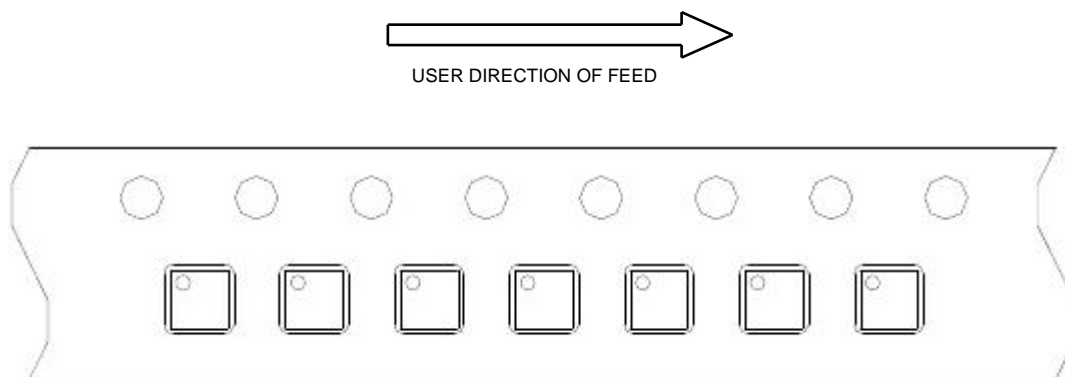
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## Devices Per Unit

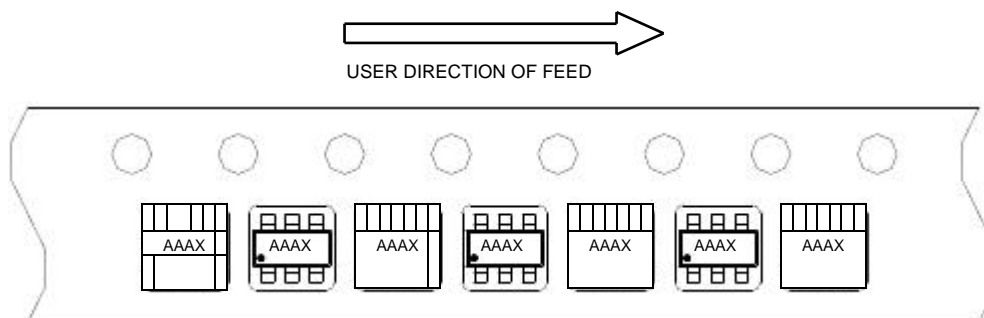
Package Type	Unit	Quantity
TDFN2x2-8	Tape & Reel	3000
TSOT-23-6A	Tape & Reel	3000

## Taping Direction Information

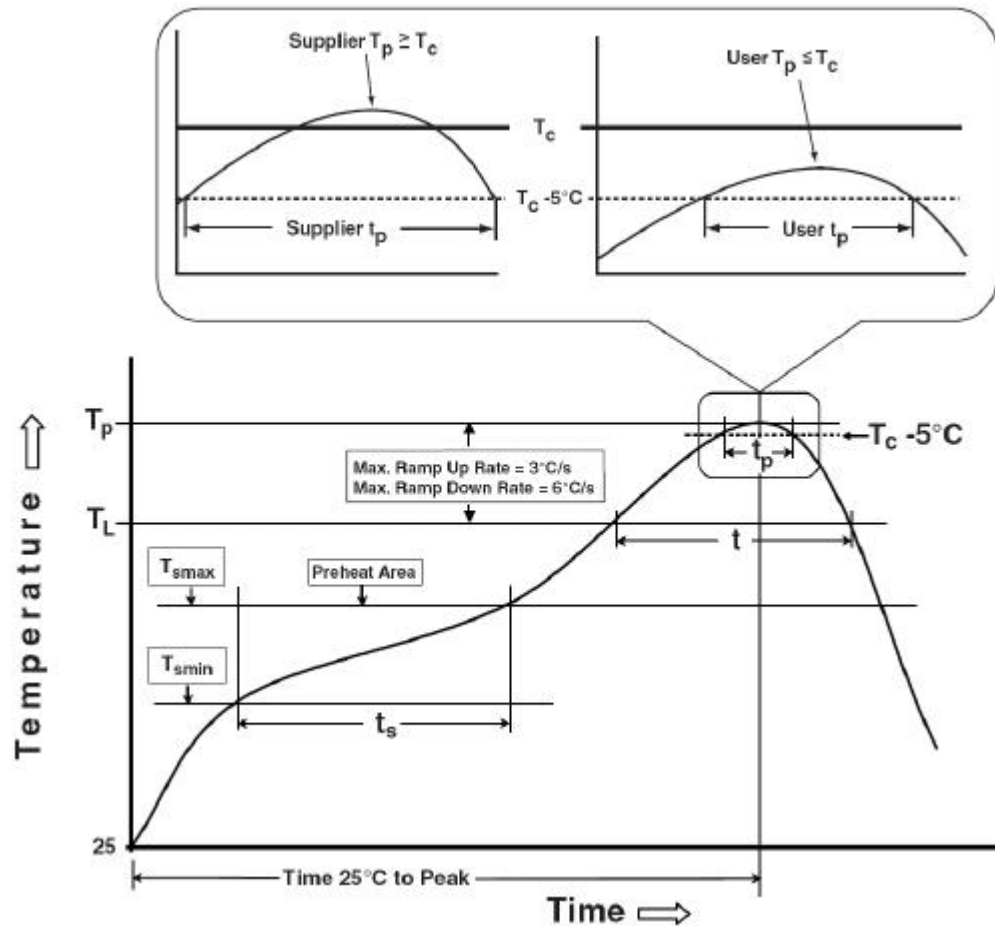
TDFN2x2-8



TSOT-23-6A



## Classification Profile



## Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
<b>Preheat &amp; Soak</b>		
Temperature min ( $T_{smin}$ )	100 °C	150 °C
Temperature max ( $T_{smax}$ )	150 °C	200 °C
Time ( $T_{smin}$ to $T_{smax}$ ) ( $t_s$ )	60-120 seconds	60-120 seconds
Average ramp-up rate ( $T_{smax}$ to $T_p$ )	3 °C/second max.	3°C/second max.
Liquidous temperature ( $T_l$ )	183 °C	217 °C
Time at liquidous ( $t_l$ )	60-150 seconds	60-150 seconds
Peak package body Temperature ( $T_p$ )*	See Classification Temp in table 1	See Classification Temp in table 2
Time ( $t_p$ )** within 5°C of the specified classification temperature ( $T_c$ )	20** seconds	30** seconds
Average ramp-down rate ( $T_p$ to $T_{smax}$ )	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature ( $T_p$ ) is defined as a supplier minimum and a user maximum.		
** Tolerance for time at peak profile temperature ( $t_p$ ) is defined as a supplier minimum and a user maximum.		

# Classification Reflow Profiles

Table 1. SnPb Eutectic Process – Classification

Temperatures (Tc)

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> 350-2000
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

## Reliability Test Program

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> 350-2000	Volume mm <sup>3</sup> >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≥ 2KV
MM	JESD-22, A115	VMM ≥ 200V
Latch-Up	JESD 78	10ms, 1 <sub>tr</sub> ≥ 100mA