Galvanically Isolated Current Sensor IC With Differential Output and Externally Adjustable Gain

FEATURES AND BENEFITS

- Fully differential architecture for improved immunity to offset drift and common mode noise
- Spare differential back end amplifier for externally adjustable gain and bandwidth using simple RC networks
- Greatly improved bandwidth through proprietary amplifier and filter design techniques
- High bandwidth 120 kHz analog output
- Patented integrated digital temperature compensation circuitry allows nearly closed-loop accuracy, through entire temperature range, in an open loop sensor
- 1.1 mΩ primary conductor resistance for low power loss and high inrush current withstanding capability
- Small footprint, low-profile QSOP24 package suitable for space-constrained applications
- Integrated shield virtually eliminates capacitive coupling from current conductor to die due to high dV/dt voltage transients

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Package: 24-pin QSOP (suffix LF)

Approximate scale

DESCRIPTION

The Allegro™ ACS726 current sensor IC family provides economical and precise solutions for AC current sensing in industrial, commercial, and communications systems. The device package allows for easy implementation by the customer. Typical applications include motor control, load detection and management, switched-mode power supplies, and overcurrent fault protection.

The fully differential output gives superior immunity to output offset drift as well common mode noise.

ACS726 is the first current sensor IC to include a fully differential back-end amplifier (BEA) that can be used to adjust gain and bandwidth via external RC networks. The BEA is fully independent and when unused, it can be powered down to reduce power consumption.

The device consists of a precise, low-offset, linear Hall sensor circuit with a copper conduction path located near the surface of the die. Applied current flowing through this copper conduction path generates a magnetic field which is sensed by the integrated Hall IC and converted into a proportional voltage. Device accuracy is optimized through the close proximity of the magnetic field to the Hall transducer. A

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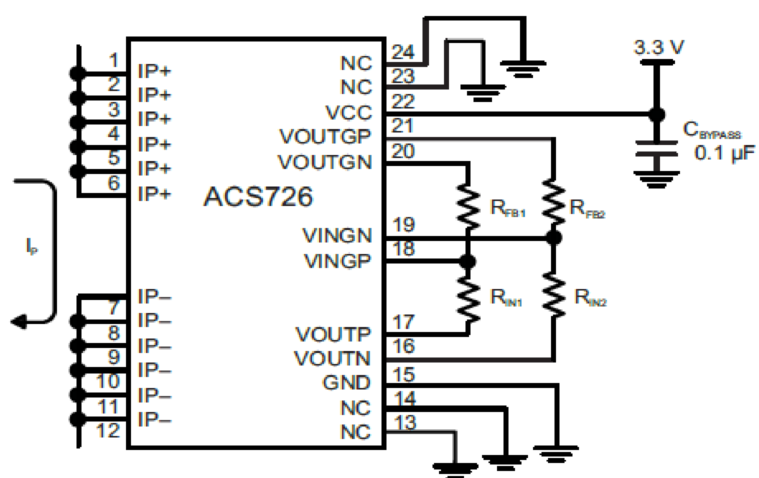


Typical Application

Current sensor IC gain can be set using RFB and RIN

Features and Benefits (continued)

- 3 to 3.6 V, single supply operation
- Factory-trimmed sensitivity and quiescent output voltage for improved accuracy
- Chopper stabilization results in extremely stable quiescent output voltage
- Ratiometric output from supply voltage

Description (continued)

precise, proportional voltage is provided by the low-offset, chopper-stabilized BiCMOS Hall IC, which is programmed for accuracy after packaging. The output of the device has a positive differential voltage ($V_{OUTP} – V_{OUTN}$) when an increasing current flows through the primary copper conduction path (from pins 1 through 6, to pins 7 through 12), which is the path used for current sensing. The internal resistance of this conductive path is 1.1 mΩ typical, providing low power loss.

The terminals of the conductive path are electrically isolated from the sensor IC signal leads (pins 13 through 24). This allows the ACS726 current sensor IC to be used in high-side current sense applications without the use of high-side differential amplifiers or other costly isolation techniques.

The ACS726 is provided in a small, low-profile surface mount QSOP24 package (suffix LF). The leadframe is plated with 100% matte tin, which is compatible with standard lead (Pb) free printed circuit board assembly processes. Internally, the device is Pb-free, except for flip-chip high-temperature Pb-based solder balls, currently exempt from RoHS. The device, excluding the BAE, is fully calibrated prior to shipment from the factory.

Selection Guide

Part Number	Optimized Range for Sensed Current, I_P (A)	Linear Range for Sensed Current, I_P (A)	Sensitivity, Sens (Typ) (mV/A)[1]	Operating Ambient Temperature Range T_A, (°C)	Packing[2]
ACS726LLFTR-20B-T[3]	±20	±20	100	–40 to 150	Tape and reel, 2500 pieces per 13-in. reel
ACS726LLFTR-40B-T[3]	±40	±40	50		

1 Measured differently when V_{CC} = 3.3 V and using a 2000 mV dynamic range.

2 Contact Allegro™ for additional packing options.

3 Variant not intended for automotive applications.

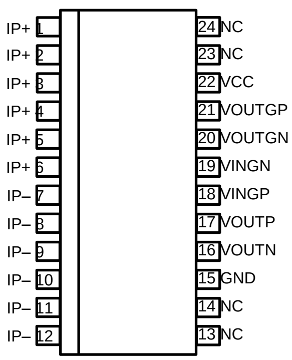
Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}	VCC pin	6	V
Reverse Supply Voltage	V_{RCC}	VCC pin	–0.1	V
Output Voltage	V_{OUTP} , V_{OUTN}	VOUTP and VOUTN pins	6	V
Reverse Output Voltage	V_{ROUTP}, V_{ROUTN}	VOUTP and VOUTN pins	–0.1	V
BEA Input Voltage	V_{INGP}, V_{INGIN}	VINGP and VINGIN pins	6	V
BEA Reverse Input Voltage	V_{RINGP} , V_{RINGN}	VINGP and VINGN pins	–0.1	V
BEA Output Voltage	V_{OUTGP} , V_{OUTGN}	VOUTGP and VOUTGN pins	6	V
BEA Reverse Output Voltage	V_{ROUTGP} , V_{ROUTGN}	VOUTGP and VOUTGN pins	–0.1	V
Output Source Current	$I_{OUT(SOURCE)}$	VOUTP, VOUTN, VOUTGP, VOUTGN pins to GND	3	mA
Output Sink Current	$I_{OUT(SINK)}$	VCC pin to VOUTP, VOUTN, VOUTGP, VOUTGN	10	mA
Electric Strength Test Voltage	V_{ESTV}	Between pins 1-12 and 13-24; 60 Hz, 1 minute (Agency Type Test), T_A = 25°C	2100	VAC
Working Voltage	$V_{working}$	For single protection according to UL 1577 standard; for higher continuous voltage ratings, please contact Allegro	277	VAC
			391	V_{pk} or VDC
Operating Ambient Temperature	T_A	Range L	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

Thermal Characteristics may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	On Allegro ACS726 evaluation board (expected value)	27	ºC/W
*Additional thermal information available on the Allegro website.				

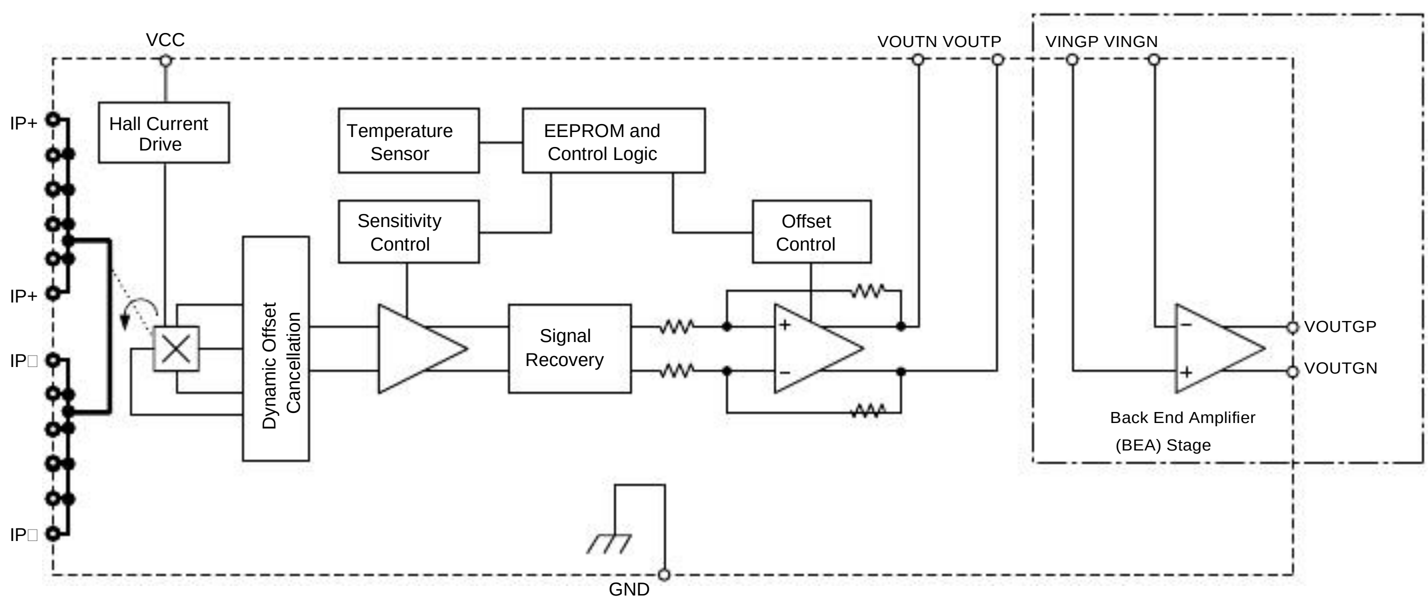
Pin-out Diagram and Terminal List Table



Package LF, 24-Pin QSOP Pin-out Diagram

Terminal List Table

Number	Name	Function
1 through 6	IP+	Terminals for current being sensed; fused internally
7 through 12	IP–	Terminals for current being sensed; fused internally
15	GND	Signal ground terminal
16	VOUTN	Negative analog output
17	VOUTP	Positive analog output
18	VINGP	Gain stage positive analog input
19	VINGN	Gain stage negative analog input
20	VOUTGN	Gain stage negative analog output
21	VOUTGP	Gain stage positive analog output
22	VCC	Device power supply terminal
13,14,23,24	NC	No Connection; connect to GND for optimal ESD performance



Functional Block Diagram

COMMON OPERATING CHARACTERISTICS: not including BEA, T_A= –40°C to 150°C, V_{CC} = 3.3 V, C_{BYPASS} = 0.1 µF; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		3	3.3	3.6	V
Supply Output Impedance	V_{CCIMP}		–	–	5	Ω
Supply Current	I_{CC}	V_{CC} = 3.3 V, no output load, BEA disabled	8	14	23	mA
	ICC_{TOTAL}	V_{CC} = 3.0 V to 3.6 V, BEA Enabled	12	22	40	mA
Output Capacitive Load	C_L	VOUTP to GND, VOUTN to GND	–	–	4.7	nF
Output Resistive Load	R_L	VOUTP to GND, VOUTN to GND	4.7	–	–	kΩ
Primary Conductor Resistance	$R_{primary}$	T_A = 25°C	–	1.1	–	mΩ
Rise Time[1]	t_r	I_P = $I_{P(MAX)}$; T_A = 25°C, C_L = 1 nF	–	3.7	–	µs
Propagation Delay[1]	t_{pd}	I_P = $I_{P(MAX)}$; T_A = 25°C, C_L = 1 nF	–	2.5	–	µs
Response Time[1]	$t_{RESPONSE}$	I_P = $I_{P(MAX)}$; T_A = 25°C, C_L = 1 nF, 90% input to 90% $V_{IOUTdiff}$	–	5	–	µs
Internal Bandwidth[1]	BW_i	Small signal –3 dB; T_A = 25°C, C_L = 1 nF	–	120	–	kHz
Linearity Error[1]	Err_{LIN}	Across full range of I_P	-1	< 0.5	1	%
Saturation Voltage	$V_{SAT(H)}$	T_A = 25°C, R_L = 4.7 kΩ to GND	V_{CC} – 0.3	–	–	V
	$V_{SAT(L)}$	T_A = 25°C, R_L = 4.7 kΩ to VCC	–	–	0.3	V
Power-On Time[1]	t_{PO}	T_A = 25°C, I_P = I_P(MAX)	–	85	–	µs
Differential Quiescent Output Voltage	$V_{IOUTdiff(Q)}$	I_P = 0	–	0	–	V
Common Mode Output Voltage[1]	V_{CMO}	I_P = 0, no load, V_{CC} = 3.3 V, T_A = 25°C to 150°C	1.4	1.65	1.9	V
Common Mode Offset Voltage	V_{CMOE}	I_P = 0, no load, V_{CC} = 3.3 V, T_A = 25°C to 150°C	-250	20	250	mV
Common Mode Output Voltage Ratiometry[1]	ΔV_{CMORAT}	T_A = 25C, V_{CC} = 3.3 V +/-10%	–	100	–	%
Sensitivity Ratiometry[1]	$\Delta Sens_{RAT}$	T_A = 25C, V_{CC} = 3.3 V +/-10%	–	100	–	%

1See Characteristic Definitions section.

ACS726-20B OPERATING CHARACTERISTICS: not including BEA, T_A= –40°C to 150°C, V_{CC} = 3.3 V, C_{BYPASS} = 0.1 µF; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Current Sensing Range	I_P		–20	–	20	A
Differential Sensitivity[1]	$Sens_{diff}$	Across full range of I_P , T_A = 25°C	98	100	102	mV/A
		Across full range of I_P , T_A = –40°C to 25°C, not cold trimmed	–	100	–	mV/A
		Across full range of I_P , T_A = 25°C to 150°C	97	100	103	mV/A
Sensitivity Drift Over Lifetime[2]	$\Delta Sens_{LIFE}$	T_A = -40C to 150C, shift after qualification testing	–	±1	–	%
Noise	$V_{NOISE(RMS)}$	BW_i = 120 kHz, T_A = 25°C, C_L= 1 nF to GND	–	10.5	–	mV_{RMS}
Input-Referenced Noise Density	$I_{ND(RMS)}$	BW_i ≤ 120 kHz, T_A = 25°C, C_L= 1 nF to GND	–	305	–	µA / √Hz
Zero Current Output Voltage	$V_{OUTP(Q)}$, $V_{OUTN(Q)}$	I_P = 0 A, T_A = 25°C, V_{CC} = 3.3 V	1.4	1.65	1.9	V
Differential Offset Voltage[3]	V_{OE}	T_A = 25°C	-15	±5	15	mV
		T_A = –40°C to 25°C, not cold trimmed	–	±10	–	mV
		T_A = 25°C to 150°C	-15	±5	15	mV
Offset Voltage Drift Over Lifetime[2]	ΔV_{OELIFE}	T_A = -40C to 150C, shift after qualification testing	–	±2	–	mV
Total Output Error[4,5]	Err_{TOT}	I_P = ±20 A, T_A = 25°C, BW_i = 120 kHz	-3	±1	3	%
		I_P = ±20 A, T_A = –40°C to 25°C, BW_i = 120 kHz, not cold trimmed	–	±2	–	%
		I_P = ±20 A, T_A = 25°C to 150°C, BW_i = 120 kHz	-3	±1	3	%
Total Output Error Drift Over Lifetime[2]	$\Delta Err_{TOTLIFE}$	T_A = -40C to 150C, shift after qualification testing	–	±1	–	%

1 This parameter may drift a maximum of $\Delta Sens_{LIFE}$ over lifetime.
2 Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits. Cannot be guaranteed. Drift is a function of customer application conditions. Please contact Allegro MicroSystems for further information.
3 This parameter may drift a maximum of ΔV_{OELIFE} over lifetime.
4 This parameter may drift a maximum of $\Delta Err_{TOTLIFE}$ over lifetime.
5 Measured as a percentage of a 2000 mV dynamic range.

ACS726-40B OPERATING CHARACTERISTICS: not including BEA, T_A= –40°C to 150°C, V_{CC} = 3.3 V, C_{BYPASS} = 0.1 µF; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Current Sensing Range	I_P		–40	–	40	A
Differential Sensitivity[1]	$Sens_{diff}$	Across full range of I_P , T_A = 25°C	49	50	51	mV/A
		Across full range of I_P , T_A = –40°C to 25°C, not cold trimmed	–	50	–	mV/A
		Across full range of I_P , T_A = 25°C to 150°C	48.5	50	51.5	mV/A
Sensitivity Drift Over Lifetime[2]	$\Delta Sens_{LIFE}$	T_A = -40C to 150C, shift after qualification testing	–	±1	–	%
Noise	$V_{NOISE(RMS)}$	BW_i = 120 kHz, T_A = 25°C, C_L= 1 nF to GND	–	5.25	–	mV_{RMS}
Input-Referenced Noise Density	$I_{ND(RMS)}$	BW_i ≤ 120 kHz, T_A = 25°C, C_L= 1 nF to GND	–	305	–	µA / √Hz
Zero Current Output Voltage	$V_{OUTP(Q)}$, $V_{OUTN(Q)}$	I_P = 0 A, T_A = 25°C, V_{CC} = 3.3V	1.40	1.65	1.9	V
Differential Offset Voltage[3]	V_{OE}	T_A = 25°C	-15	±3	15	mV
		T_A = –40°C to 25°C, not cold trimmed	–	±8	–	mV
		T_A = 25°C to 150°C	-15	±3	15	mV
Offset Voltage Drift Over Lifetime[2]	ΔV_{OELIFE}	T_A = -40C to 150C, shift after qualification testing	–	±2	–	mV
Total Output Error[4,5]	Err_{TOT}	I_P = ±40 A, T_A = 25°C, BW_i = 120 kHz	-2.5	±1	2.5	%
		I_P = ±40 A, T_A = –40°C to 25°C, BW_i = 120 kHz, not cold trimmed	–	±2	–	%
		I_P = ±40 A, T_A = 25°C to 150°C, BW_i = 120 kHz	-2.5	±1	2.5	%
Total Output Error Drift Over Lifetime[2]	$\Delta Err_{TOTLIFE}$	T_A = -40C to 150C, shift after qualification testing	–	±1	–	%

1 This parameter may drift a maximum of $\Delta Sens_{LIFE}$ over lifetime.
2 Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits. Cannot be guaranteed. Drift is a function of customer application conditions. Please contact Allegro MicroSystems for further information.
3 This parameter may drift a maximum of ΔV_{OELIFE} over lifetime.
4 This parameter may drift a maximum of $\Delta Err_{TOTLIFE}$ over lifetime.
5 Measured as a percentage of a 2000 mV dynamic range.

Differential Back End Amplifier (BEA) OPERATING CHARACTERISTICS[1]: T_A= –40°C to 150°C, V_{CC} = 3.3 V, C_{BYPASS} = 0.1 µF; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Load						
Output Capacitive Load	$C_{L(BEA)}$	VOUTGP to GND, VOUTGN to GND	–	–	4.7	nF
Output Resistive Load	$R_{L(BEA)}$	VOUTGP to GND, VOUTGN to GND	4.7	–	–	kΩ
Gain Setting Resistance						
Feedback Resistor[1]	$R_{FB(BEA)}$		9.4	–	50	kΩ
Input Resistor[1]	$R_{IN(BEA)}$		4.7	–	25	kΩ
AC Performance						
Open Loop Gain	$G_{OL(BEA)}$		–	90	–	dB
Closed Loop Gain[2]	$G_{CL(BEA)}$		2	–	10	–
Bandwidth	$BW_{(BEA)}$	$G_{CL(BEA)}$ = 2, $C_{L(BEA)}$ = 1 nF	–	1000	–	kHz
Gain Bandwidth Product	$GBWP_{(BEA)}$	$C_{L(BEA)}$ = 1 nF	–	2000	–	kHz
Differential Slew Rate	$SR_{D(BEA)}$	$G_{CL(BEA)}$ = 2, $C_{L(BEA)}$ = 1 nF	–	1.5	–	V/µs
Settling Time to 1%	$t_{S(BEA)}$	$G_{CL(BEA)}$ = 2, $C_{L(BEA)}$ = 1 nF, V_{OUTGP} – V_{OUTGN} = 100 mV	–	3	–	µs
Input-Referred Voltage Noise Density	$V_{ND(BEA)}$	T_A = 25°C, $BW_{(BEA)}$ < 120 kHz, $G_{CL(BEA)}$ = 2	–	40	–	nV/ √Hz
DC Performance						
Input-Referred Differential Offset Voltage	$V_{OEIR(BEA)}$	At T_A = 25°C	-7	±3	7	mV
		At T_A = 25°C to 150°C	-7	±3	7	mV
Quiescent Operating Current[3]	$I_{Q(BEA)}$	$G_{CL(BEA)}$ = 2, $C_{L(BEA)}$ = 1 nF	3.5	7	17	mA
Power Supply Rejection Ratio	$PSRR_{(BEA)}$	$G_{CL(BEA)}$ = 2, $C_{L(BEA)}$ = 1 nF, $BW_{(BEA)}$ < 1 kHz	–	-70	–	dB
Input						
Minimum Common Mode Input Range	$V_{CMIRMIN}$ (BEA)	V_{CC} = 3.3 V, $G_{CL(BEA)}$ = 2, $RIN_{(BEA)}$ = 4.7 K, $RFB_{(BEA)}$ = 9.4 K	1	–	–	V
	$V_{CMIRMAX}$ (BEA)	V_{CC} = 3.3 V, $G_{CL(BEA)}$ = 2, $RIN_{(BEA)}$ = 4.7 K, $RFB_{(BEA)}$ = 9.4 K	–	–	2.15	V
Common Mode Rejection Ratio	$CMRR_{(BEA)}$	$G_{CL(BEA)}$ = 2, $C_{L(BEA)}$ = 1 nF, $BW_{(BEA)}$ < 1 kHz	–	60	–	dB
Input Bias Current	$I_{bias(BEA)}$	V_{CC} = 3.3 V, VINGP = VINGN = 1.65 V	-1.5	<1	1.5	µA
Output						
Saturation Voltage	$V_{SAT(H)(BEA)}$	T_A = 25°C, $R_{L(BEA)}$ = 4.7 kΩ to GND	V_{CC} – 0.3	–	–	V
	$V_{SAT(L)(BEA)}$	T_A = 25°C, $R_{L(BEA)}$ = 4.7 kΩ to VCC	–	–	0.3	V
Common Mode Output Voltage	$V_{CMO(BEA)}$	V_{CC} = 3.3 V, G_{CL} = 2, T_A = 25°C to 150°C	1.4	1.65	1.9	V
Common Mode Offset Voltage	$V_{CMOE(BEA)}$	V_{CC} = 3.3 V, G_{CL} = 2, T_A = 25°C to 150°C	-250	±20	250	mV
DC Output Resistance	$R_{OUT(BEA)}$		–	<1	–	Ω
Linearity	$Err_{Lin(BEA)}$	$G_{CL(BEA)}$ = 2, Over 2 V differential dynamic range	–	<±0.1	–	%

[1] If larger resistor values are used, settling time deteriorates. Adding a capacitor in parallel with the feedback resistor improves settling time.
[2] Allegro does not guarantee BAE performance and stability for Closed Loop Gain outside the recommended range.
[3] The Back End Amplifier can be powered-down by connecting VINGP and VINGN to GND, causing VOUTGP and VOUTGN to be = Vcc/2

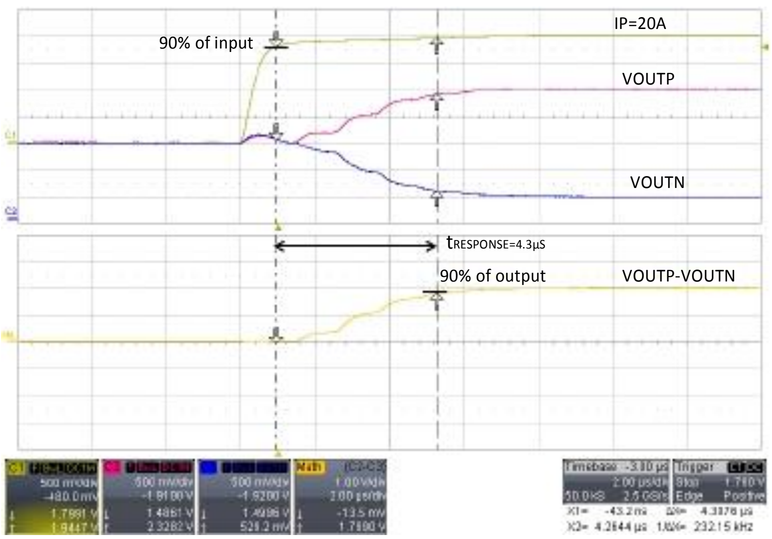
CHARACTERISTIC PERFORMANCE DATA

Data taken using the ACS726LLFTR-20B-T

Timing Data

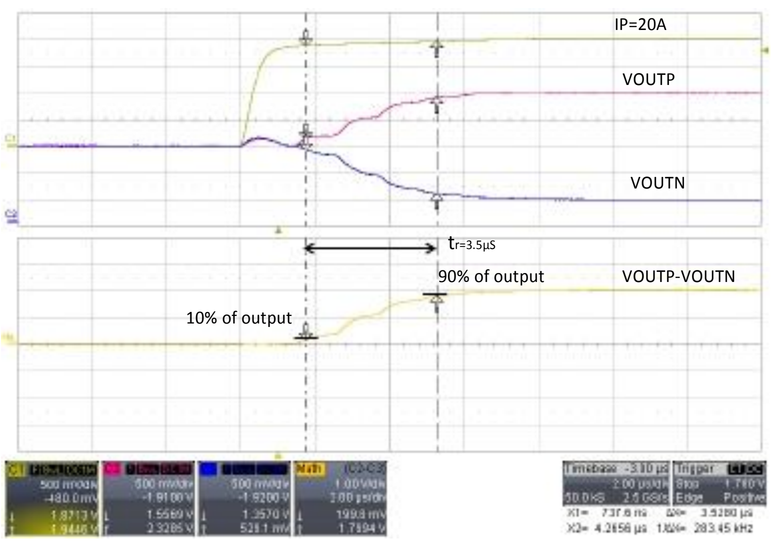
Response Time (90%input-90%output)

IP=20 A, 10% to 90% IP rise time < 1 μS, CBYPASS = 0.1 μF, CL =1 nF from VOUTP to GND and VOUTN to GND



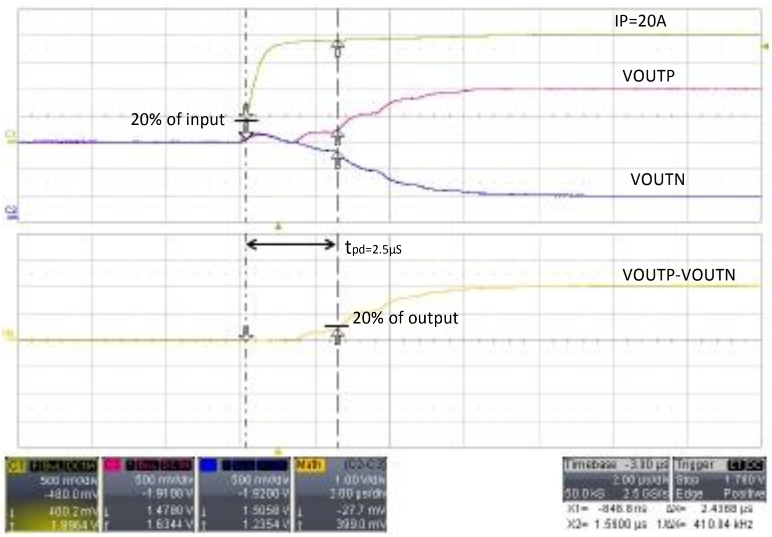
Rise Time (10%output-90%output)

IP=20 A, 10% to 90% IP rise time < 1 μS, CBYPASS = 0.1 μF, CL = 1 nF from VOUTP to GND and VOUTN to GND



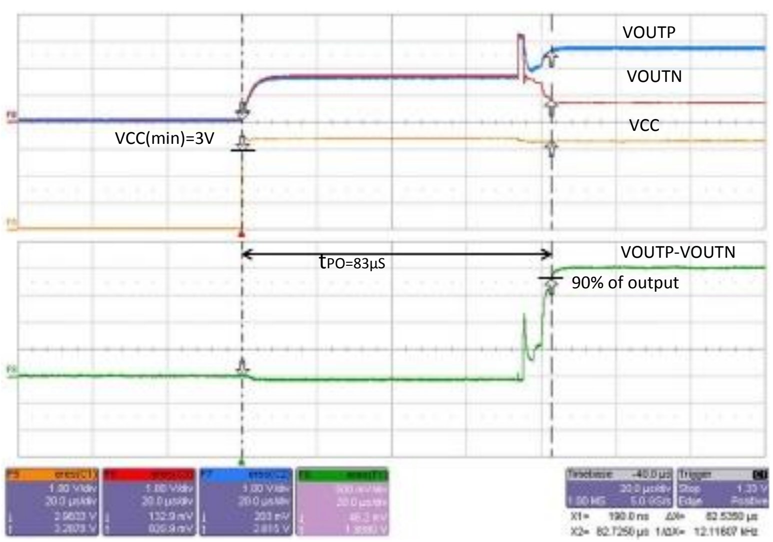
Propagation Delay(20%input-20%output)

IP = 20 A, 10% to 90% IP rise time < 1 µS, CBYPASS = 0.1 µF, CL = 1 nF from VOUTP to GND and VOUTN to GND



Power-On Time

IP = 20 A, 10% to 90% rise time < 1 µS



CHARACTERISTICS DEFINITIONS

Accuracy Characteristics

Differential Sensitivity ($Sens_{diff}$) The change in the differential sensor IC output ($V_{OUTP} – V_{OUTN}$) in response to a 1A change through the primary conductor. The sensitivity is the product of the magnetic circuit sensitivity (G /A) (1 G = 0.1 mT) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is programmed at the factory to optimize the sensitivity (mV/A) for the full-scale current of the device.

Noise ($V_{NOISE(RMS)}$) The unfiltered output noise of the current sensor IC. Dividing the noise (mV) by the sensitivity (mV/A) provides the smallest current that the device is able to resolve.

Linearity Error (Err_{LIN})* The ACS726 is designed to provide a linear output in response to a ramping current. Consider two current levels, I1 and I2. Ideally, the sensitivity of a device is the same for both currents, for a given supply voltage and temperature. Nonlinearity is present when there is a difference between the sensitivities measured at I1 and I2. Nonlinearity is calculated separately for the positive ($Err_{LIN\,pos}$) and negative (Err_{LINneg}) applied currents as follows:

$$Err_{LINpos} = 100(\%) \times \left\{ - \left(1 \quad \frac{Sens_{IPOS2}}{Sens_{IPOS1}} \right) \right\}$$

$$Err_{LINneg} = 100(\%) \times \left\{ - \left(1 \quad \frac{Sens_{INEG2}}{Sens_{INEG1}} \right) \right\}$$

where:

$Sens_{Ix} = (V_{IOUTdiff(Ix)} – V_{IOUTdiff(Q)})/ Ix$ and $IPOS_x$ and $INEG_x$ are positive and negative currents. Then:

$Err_{LIN} = max(Err_{LINpos}, Err_{LINneg})$

Differential Quiescent Output Voltage ($V_{IOUTdiff(Q)}$)* The differential output of the sensor IC when the primary current is zero. It is nominally 0 V.

Differential Offset Voltage (V_{OE}) The deviation of the device output, from its ideal quiescent value of 0 V, due to nonmagnetic causes. To convert this voltage to amperes, divide by the device sensitivity, Sens.

Common Mode Output Voltage (V_{CMO}) The average of the positive and negative zero current output voltages: ($V_{OUTP(Q)}$ + $V_{OUTN(Q)}$) / 2. V_{CMO} nominally equals V_{CC} / 2.

Common Mode Offset Voltage (V_{CMOE}) The deviation of the Common Mode Output Voltage from its ideal value of V_{CC} / 2.

Total Output Error (ETOT)* The maximum deviation of the actual output from its ideal value, also referred to as accuracy, illustrated graphically in the Output voltage versus Sensed current chart .

ETOT is divided into four areas:

0 A at 25 ℃. Accuracy at the zero current flow at 25 ℃, without the effects of temperature.

0 A over Δ temperature. Accuracy at the zero current flow including temperature effects.

Full-scale current at 25 ℃. Accuracy at the full-scale current at 25 ℃, without the effects of temperature.

Full-scale current over Δ temperature. Accuracy at the fullscale current flow including temperature effects.

$$E_{TOT(IP)} = 100(\%) \times \left| \frac{(V_{IOUTdiff(Ip)} - V_{IOUTdiff\_IDEAL(Ip)})}{Sens_{diff\_IDEAL} \times IP} \right|$$

Where

$V_{IOUTdiff\_IDEAL(IP)} = V_{IOUTdiff\_IDEAL(Q)} + (Sens_{diff\_IDEAL} \times Ip)$

The Total Output Error incorporates all sources of error and is a function of I_P. At relatively high currents, E_{TOT} will be mostly due to sensitivity error, and at relatively low currents, E_{TOT} will be mostly due to Offset Voltage (V_{OE}). In fact, at I_P = 0, E_{TOT} approaches infinity due to the offset.

This is illustrated in the total output error versus sensed current chart.

Ratiometry The ratiometric feature means that the Common Mode Output Voltage, V_{CMO} , and Differential Sensitivity, $Sens_{diff}$, are proportional to the supply voltage, V_{CC} . The following formula is used to derive the ratiometric change in common mode 0 A output voltage, $\otimes V_{CMORAT}$ (%).

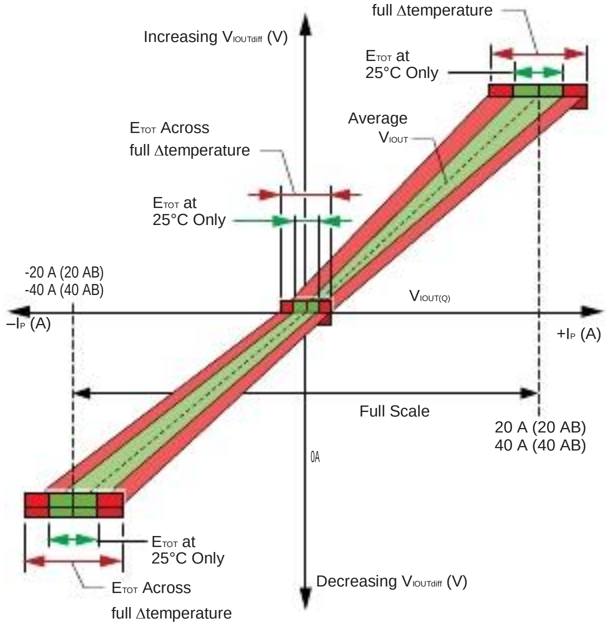
$$100 \; \frac{V_{CMO(VCC)} / V_{CMO(3.3V)}}{V_{CC} / 3.3\text{ V}}$$

The ratiometric change in sensitivity, $\otimes Sens_{RAT}$ (%), is defined as:

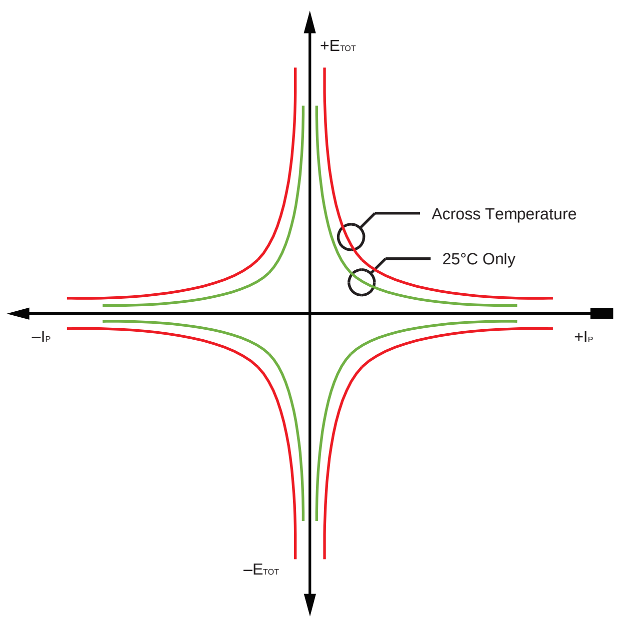
$$100 \; \frac{Sens_{diff(VCC)} / Sens_{diff(3.3V)}}{V_{CC} / 3.3\text{ V}}$$

*Definitions of V_{IOUT}:
· $V_{IOUTdiff} = V_{OUTP} – V_{OUTN}$
· $V_{IOUTdiff(Q)} = V_{OUTP(Q)} – V_{OUTN(Q)}$; sensed current equals 0 A

Output Voltage versus Sensed Current
Total Output Error at 0 A and at Full-Scale Current



Total Output Error versus Sensed Current



Dynamic Response Characteristics

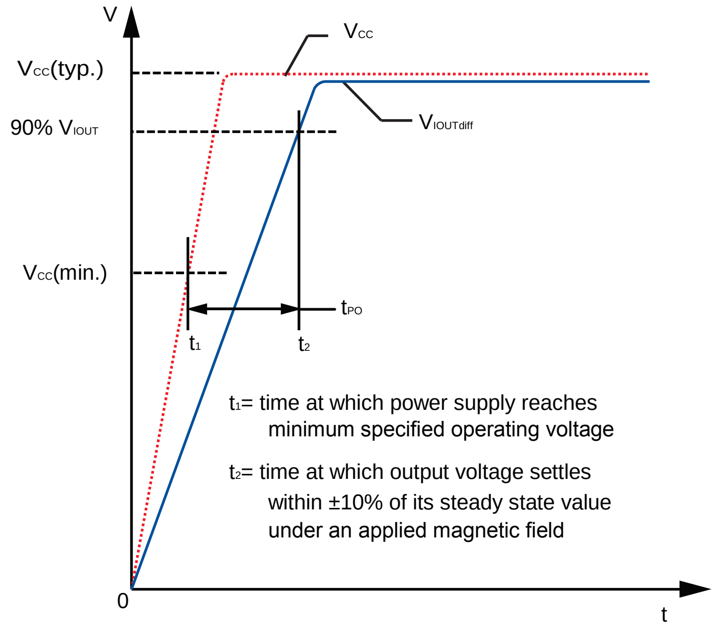
Power-On Time (t_{PO}). When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field. Power-On Time, t_{PO} , is defined as the time it takes for the output voltage to settle within ±10% of its steady state value when full scale I_P is applied, after the power supply has reached its minimum specified operating voltage, V_{CC}(min), as shown in the chart at right.

Rise Time (t_r) The time interval between a) when the sensor IC differential output reaches 10% of its full scale value, and b) when it reaches 90% of its full scale value.

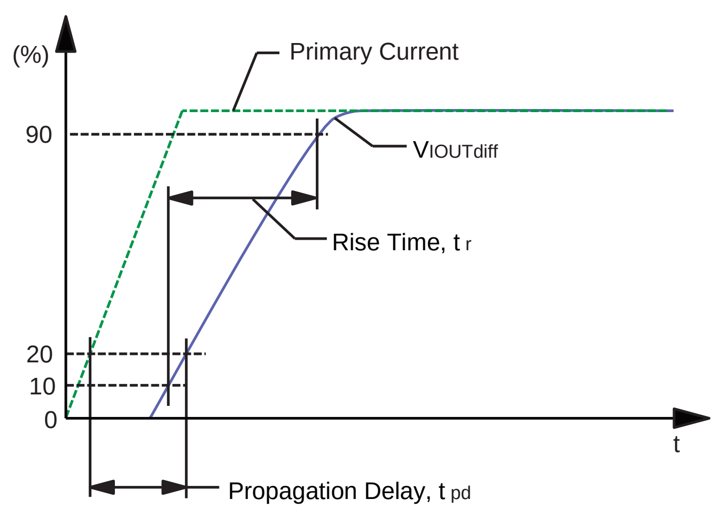
Propagation Delay (t_{pd}) The time interval between a) when the input current reaches 20% of it's final value, and b) when the differential output reaches 20% of its final value.

Response Time ($t_{RESPONSE}$) The time interval between a) when the applied current reaches 90% of its final value, and b) when the sensor differential output reaches 90% of its final value corresponding to the applied current.

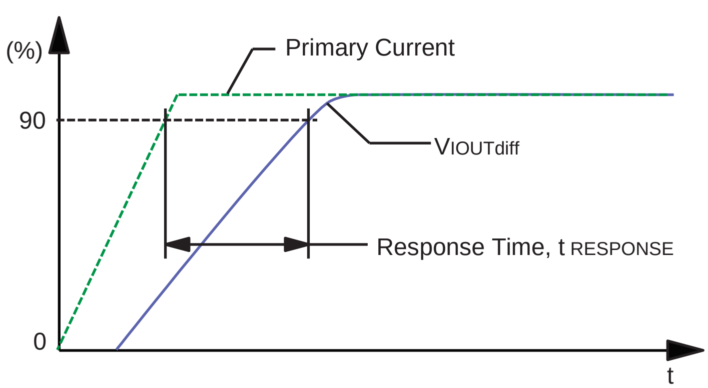
Power-On Time



Rise Time and Propagation Delay



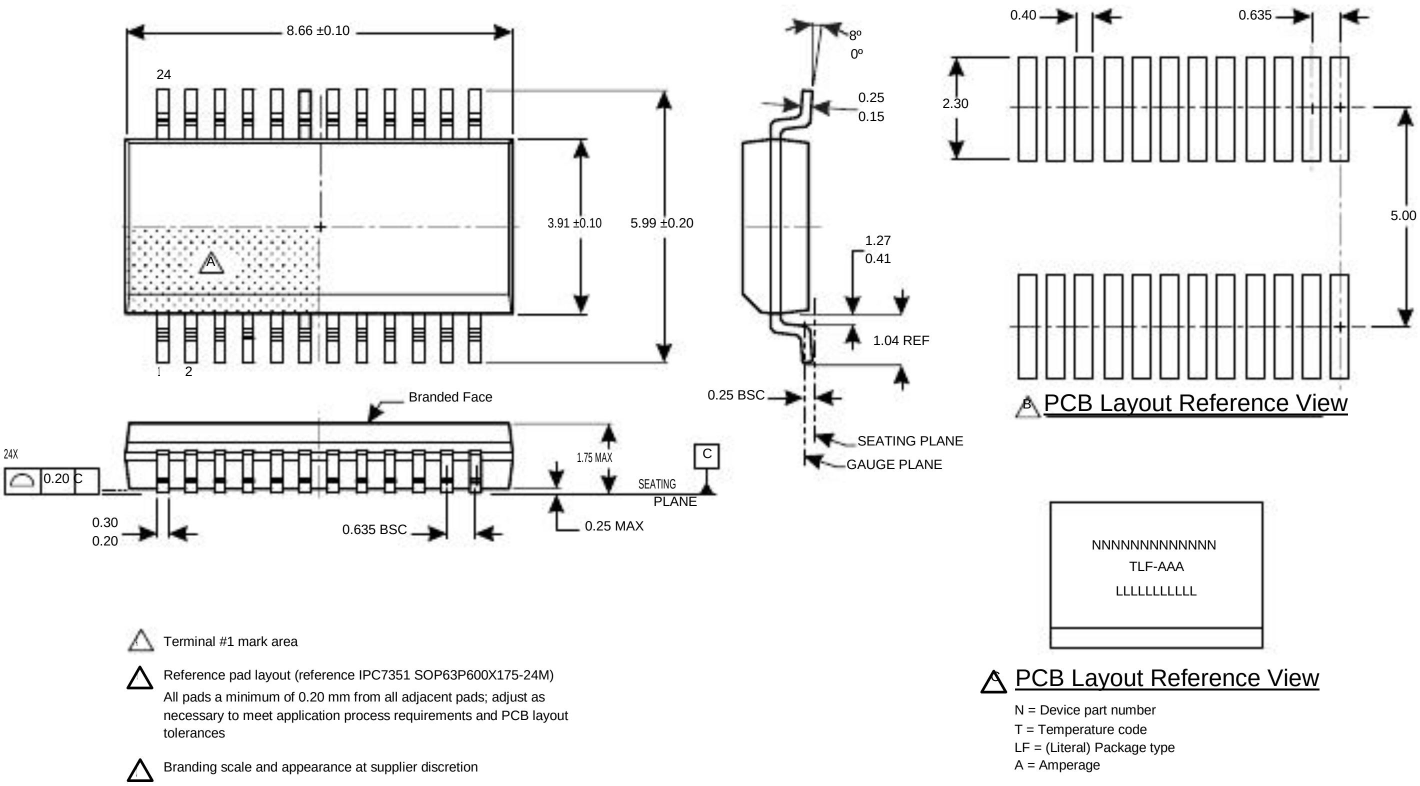
Response Time



PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-137 AE)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



Package LF, 24-Pin QSOP

Document Revision History

Revision	Date	Change
–	April 3, 2014	Initial release
1	August 13. 2014	Removed “A” deisgnator from part number and reformatted document