

JTM3420D

2A, 2.3V-6V Input, 1.5MHz Synchronous Step-Down Converter

FEATURES

- High Efficiency: Up to 96%
- 1.5MHz Constant Frequency Operation
- 2A Output Current
- No Schottky Diode Required
- 2.3V to 6V Input Voltage Range
- Output Voltage as Low as 0.6V
- PFM Mode for High Efficiency in Light Load
- 100% Duty Cycle in Dropout Operation
- Low Quiescent Current: 40 μ A
- Short Circuit Protection
- Thermal Fault Protection
- Inrush Current Limit and Soft Start
- <1 μ A Shutdown Current
- DFN3X3-10 package

APPLICATIONS

- Cellular and Smart Phones
- Wireless and DSL Modems
- PDAs
- Portable Instruments
- Digital Still and Video Cameras
- PC Cards

GENERAL DESCRIPTION

The JTM3420D is a 1.5MHz constant frequency, current mode step-down converter. It is ideal for portable equipment requiring very high current up to 2A from single-cell Lithium-ion batteries while still achieving over 90% efficiency during peak load conditions. The JTM3420D also can run at 100% duty cycle for low dropout operation, extending battery life in portable systems while light load operation provides very low output ripple for noise sensitive applications. The JTM3420D can supply up to 2A output load current from a 2.3V to 6V input voltage and the output voltage can be regulated as low as 0.6V. The high switching frequency minimizes the size of external components while keeping switching losses low. The internal slope compensation setting allows the device to operate with smaller inductor values to optimize size and provide efficient operation. The device is available in a Pb-free, 3x3mm 10-lead DFN package and is rated over the -40°C to +85°C temperature range. This device offers two operation modes, PWM control and PFM Mode switching control, which allows a high efficiency over the wider range of the load.

TYPICAL APPLICATION

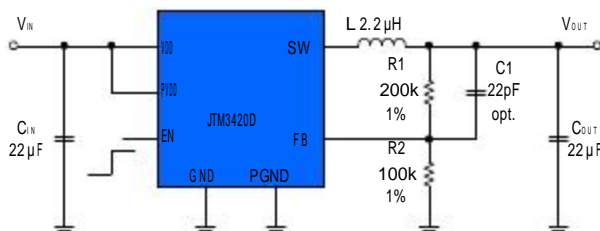
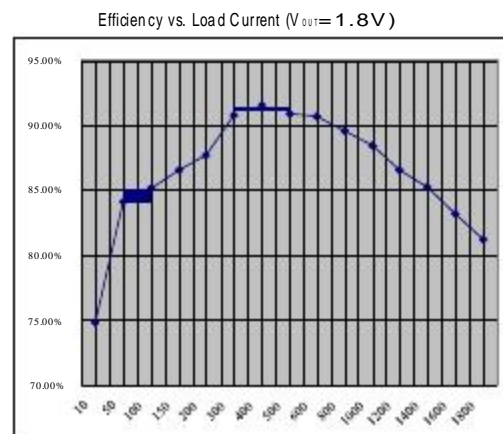


Figure 1. Basic Application Circuit

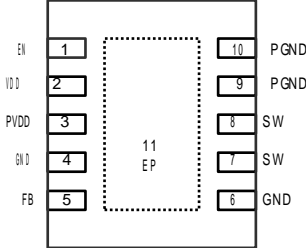


ABSOLUTE MAXIMUM RATINGS

(Note 1)

| | | | |
|--|------------------------------|---------------------------------------|----------------|
| Input Supply Voltage..... | -0.3V to 6.5V | Junction Temperature(Note2)..... | 150°C |
| EN,FB Voltages..... | -0.3V to ($V_{IN} + 0.3V$) | Operating Temperature Range..... | -40°C to 85°C |
| SW Voltage..... | -0.3V to ($V_{IN} + 0.3V$) | Lead Temperature(Soldering, 10s)..... | 300°C |
| Power Dissipation..... | 2.6W | Storage Temperature Range..... | -65°C to 150°C |
| Thermal Resistance θ_{JC} | 8°C/W | ESD HBM(Human Body Mode)..... | 2kV |
| Thermal Resistance θ_{JA} | 38°C/W | ESD MM(Machine Mode)..... | 200V |

PACKAGE/ORDER INFORMATION

| TOP VIEW | Order Part Number | Package | Top Marking |
|--|-------------------|-----------|---------------------------------------|
|  <p>3mm x 3mm, 10-Pin DFN Package $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 38^{\circ}C/W$, $\theta_{JC} = 8^{\circ}C/W$</p> | JTM3420D | DFN3X3-10 | 3420 <u>YMNNV</u> <u>FLLLLL</u> |

PIN DESCRIPTION

| Pin Name | Pin Number | Description |
|----------|------------|---|
| EN | 1 | Chip Enable Pin. Drive EN above 1.5V to turn on the part. Drive EN below 0.3V to turn it off. Do not leave EN floating. |
| VDD | 2 | Analog supply input pin. |
| PVDD | 3 | Power Supply Input. Must be closely decoupled to GND with a 10 μ F or greater ceramic capacitor. |
| GND | 4,6 | Analog ground pin. |
| FB | 5 | Output Voltage Feedback Pin. An internal resistive divider divides the output voltage down for comparison to the internal reference voltage. |
| SW | 7,8 | Power Switch Output. It is the switch node connection to Inductor. This pin connects to the drains of the internal P-ch and N-ch MOSFET switches. |
| PGND | 9,10 | Power Ground Pin. |
| EP | 11 | Power Ground exposed pad, Must be connected to bare copper ground plane. |

ELECTRICAL CHARACTERISTICS (Note 3)(V_{IN}=V_{EN}=3.6V, V_{OUT}=1.8V, T_A = 25°C, unless otherwise noted.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|-------|-------|-------|--------------------|
| Input Voltage Range | | 2.3 | | 6 | V |
| UVLO Threshold | | 1.7 | 1.9 | 2.1 | V |
| Input DC Supply Current | (Note 4) | | | | μA |
| PWM Mode | V _{OUT} = 90%, I _{LOAD} =0mA | | 150 | 300 | μA |
| PFM Mode | V _{OUT} = 105%, I _{LOAD} =0mA | | 40 | 75 | μA |
| Shutdown Mode | V _{EN} = 0V, V _{IN} =4.2V | | 0.1 | 1.0 | μA |
| Regulated Feedback Voltage V _{FB} | T _A = 25°C | 0.588 | 0.600 | 0.612 | V |
| | T _A = 0°C ≤ T _A ≤ 85°C | 0.586 | 0.600 | 0.613 | V |
| | T _A = -40°C ≤ T _A ≤ 85°C | 0.585 | 0.600 | 0.615 | V |
| Reference Voltage Line Regulation | V _{IN} =2.5V to 5.5V | | 0.1 | | %/V |
| Output Voltage Accuracy | V _{IN} = 2.5V to 5.5V, I _{OUT} =10mA to 2000mA | -3 | | +3 | % V _{OUT} |
| Output Voltage Load Regulation | I _{OUT} =10mA to 2000mA | | 0.2 | | %/A |
| Oscillation Frequency | V _{OUT} =100% | | 1.5 | | MHz |
| | V _{OUT} =0V | | 300 | | kHz |
| On Resistance of PMOS | I _{SW} =100mA | | 100 | 150 | mΩ |
| On Resistance of NMOS | I _{SW} =-100mA | | 90 | 150 | mΩ |
| Peak Current Limit | V _{IN} =3V, V _{OUT} =90% | | 4 | | A |
| EN Threshold | | 0.30 | 1.0 | 1.50 | V |
| EN Leakage Current | | | ±0.01 | ±1.0 | μA |
| SW Leakage Current | V _{EN} =0V, V _{IN} =V _{SW} =5V | | ±0.01 | ±1.0 | μA |

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

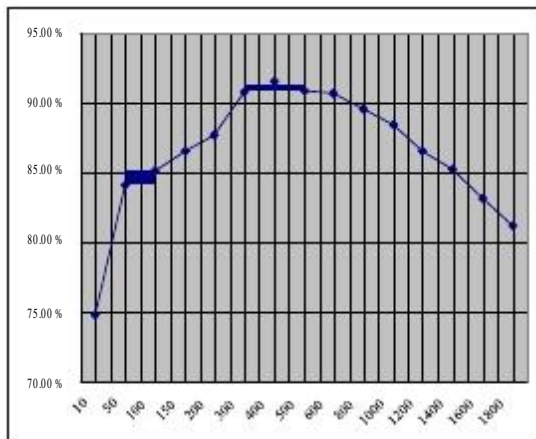
Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: T_J = T_A + (P_D) x (38°C/W).

Note 3: 100% production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

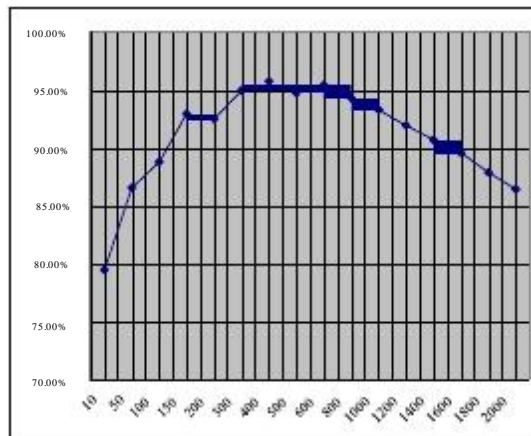
Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

TYPICAL PERFORMANCE CHARACTERISTICS

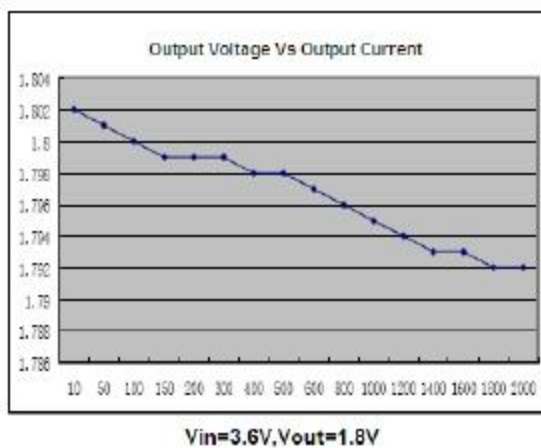
Efficiency vs. Load Current
 $V_{out}=1.8V$



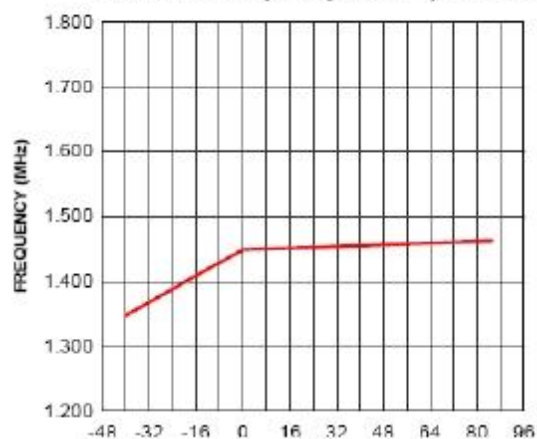
Efficiency vs. Load Current
 $V_{out}=3.3V$



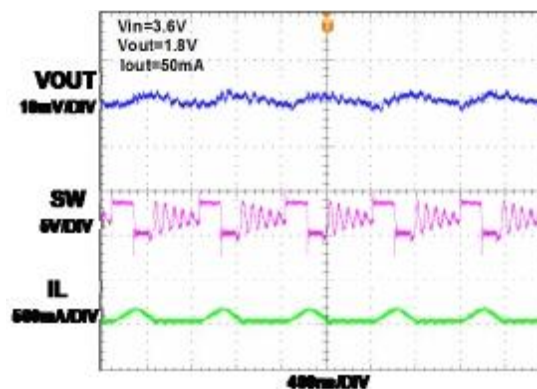
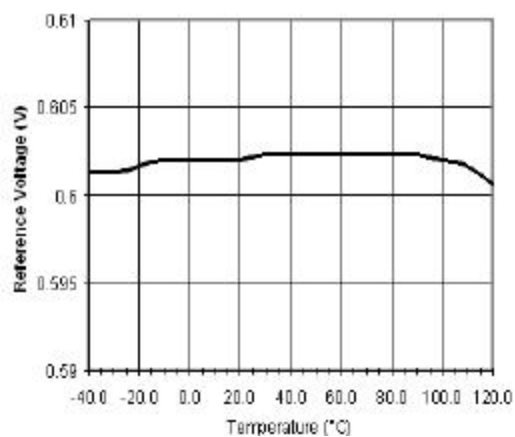
Output Voltage Vs Output Current



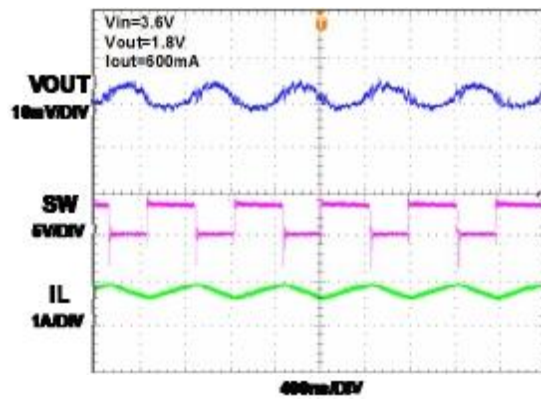
Oscillator Frequency vs Temperature



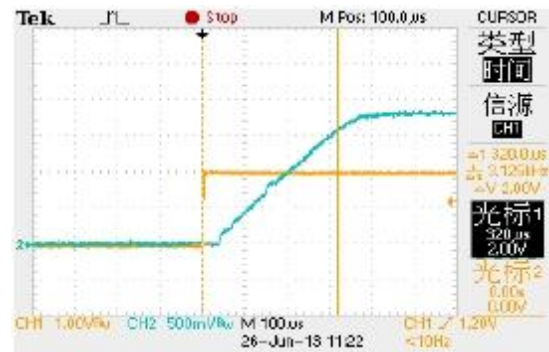
PFM MODE



PWM MODE



START UP RESPONSE



FUNCTIONAL BLOCK DIAGRAM

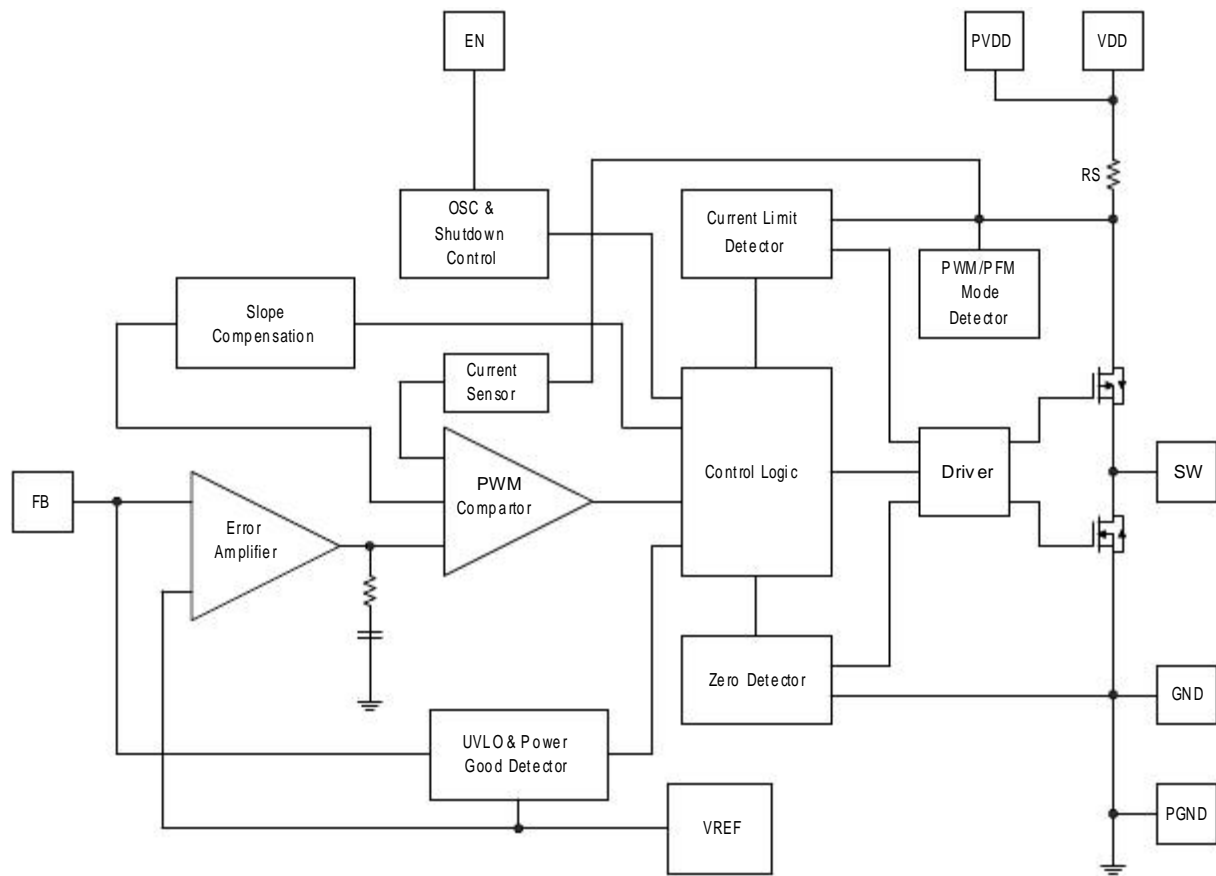


Figure 2. JTM3420D Block Diagram

FUNCTIONAL DESCRIPTION

The JTM3420D is a high output current monolithic switch mode step-down DC-DC converter. The device operates at a fixed 1.5MHz switching frequency, and uses a slope compensated current mode architecture. This step-down DC-DC converter can supply up to 2A output current at $V_{IN} = 3.6V$ and has an input voltage range from 2.3V to 6V. It minimizes external component size and optimizes efficiency at the heavy load range. The slope compensation allows the device to remain stable over a wider range of inductor values so that smaller values (1 μ H to 4.7 μ H) with lower DCR can be used to achieve higher efficiency. Only a small bypass input capacitor is required at the output. The

adjustable output voltage can be programmed with external feedback to any voltage, ranging

from 0.6V to near the input voltage. It uses internal MOSFETs to achieve high efficiency and can generate very low output voltages by using an internal reference of 0.6V. At dropout operation, the converter duty cycle increases to 100% and the output voltage tracks the input voltage minus the low $R_{DS(ON)}$ drop of the P-channel high-side MOSFET and the inductor DCR. The internal error amplifier and compensation provides excellent transient response, load and line regulation. Internal soft start eliminates any output voltage overshoot when the enable or the input voltage is applied.

Setting the Output Voltage

Figure 1 shows the basic application circuit for the JTM3420D. The JTM3420D can be externally programmed. Resistors R1 and R2 in Figure 1 program the output to regulate at a voltage higher than 0.6V. To limit the bias current required for the external feedback resistor string while

maintaining good noise immunity, the minimum suggested value for R2 is 59k Ω . Although a larger value will further reduce quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Table 1 summarizes the resistor values for various output voltages with R2 set to either 59k Ω for good noise immunity or 316k Ω for reduced no load input current.

The external resistor sets the output voltage according to the following equation:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R1}{R2} \right)$$

$$R1 = \left(\frac{V_{OUT}}{0.6} - 1 \right) \times R2$$

Table 1 shows the resistor selection for different output voltage settings.

| $V_{OUT}(V)$ | R2=59k Ω | R2=316k Ω |
|--------------|-----------------|------------------|
| | R1(k Ω) | R1(k Ω) |
| 0.8 | 19.6 | 105 |
| 0.9 | 29.4 | 158 |
| 1.0 | 39.2 | 210 |
| 1.1 | 49.9 | 261 |
| 1.2 | 59.0 | 316 |
| 1.3 | 68.1 | 365 |
| 1.4 | 78.7 | 422 |
| 1.5 | 88.7 | 475 |
| 1.8 | 118 | 634 |
| 1.85 | 124 | 655 |
| 2.0 | 137 | 732 |
| 2.5 | 187 | 1000 |
| 3.3 | 267 | 1430 |

Table 1: Resistor selections for different output voltage settings (standard 1% resistors substituted for calculated values).

APPLICATIONS INFORMATION

Inductor Selection

For most designs, the JTM3420D operates with inductors of 1μH to 4.7μH. Low inductance values are physically smaller but require faster switching, which results in some efficiency loss. The inductor value can be derived from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is inductor Ripple Current. Large value inductors result in lower ripple current and small value inductors result in high ripple current. For optimum voltage-positioning load transients, choose an inductor with DC series resistance in the 50mΩ to 150 mΩ range.

| PART NUMBER | VALUE (μH) | DCR | MAX DC | SIZE L*W*H(mm.) |
|--------------------|------------|---------|----------------|--------------------|
| | | (Ω MAX) | CURRENT (A) | |
| Sumida CDRH5D16 | 2.2 | 28.7 | 3 | 5.8x5.8x1.8 |
| | 3.3 | 35.6 | 2.6 | |
| | 4.7 | 19 | 3.4 | 8.3x8.3x3.0 |
| Sumida CDRH5D16 | 2.2 | 23 | 3.3 | 5.2x5.2x3.0 |
| | 3.3 | 29 | 2.6 | |
| | 4.7 | 39 | 2.1 | |

Table2.Recommend Surface Mount Inductors

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency should be less than input source impedance to prevent high frequency switching current passing to the input. A low ESR input capacitor sized for maximum RMS current must be used. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 22μF ceramic capacitor for most applications is sufficient. A large value may be used for improved input voltage filtering.

Output Capacitor Selection

The output capacitor is required to keep the output voltage ripple small and to ensure regulation loop stability. The output capacitor must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and high ripple current ratings. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \leq \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times 0.6 \times L} \times ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}}$$

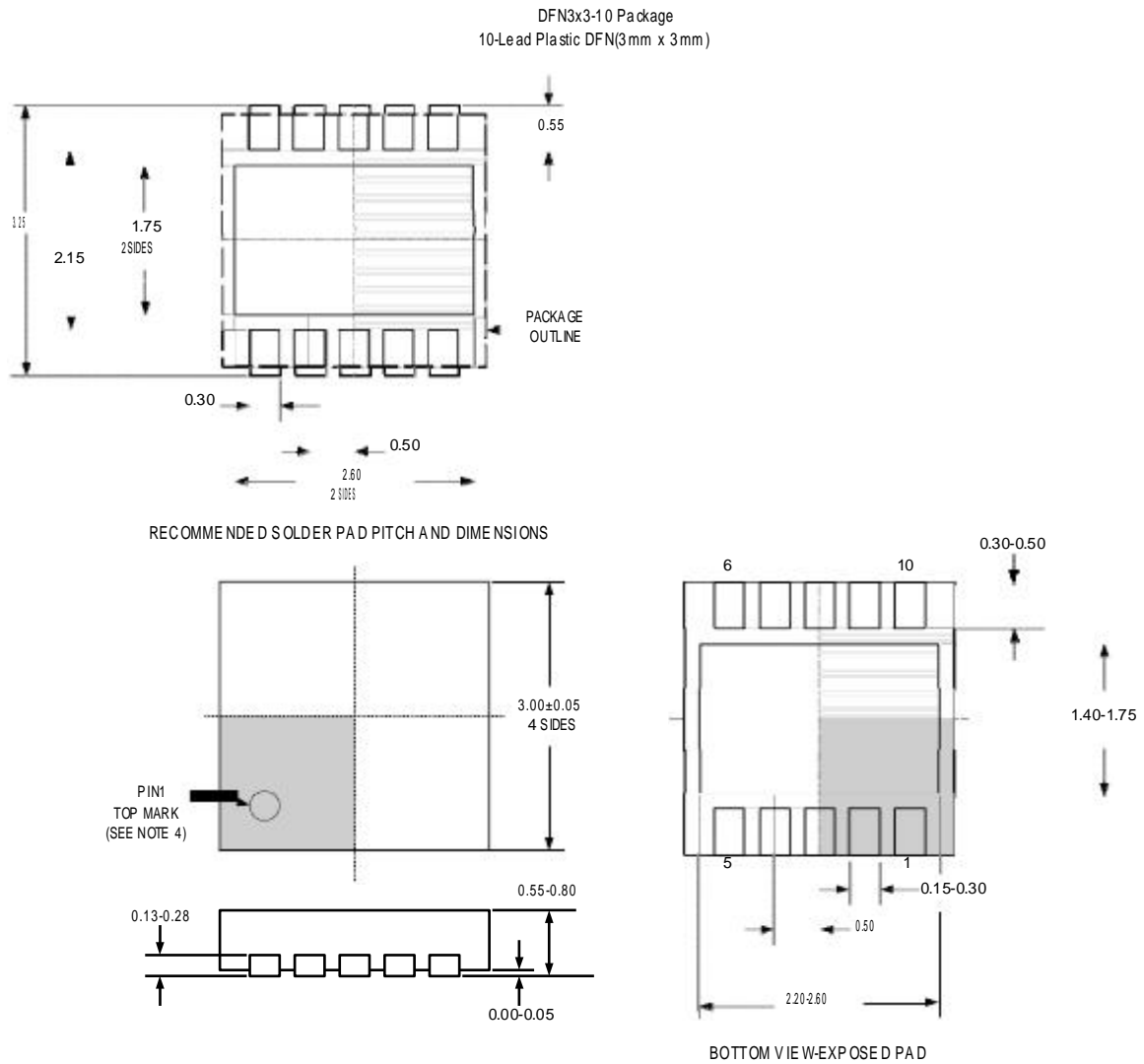
A 22μF ceramic can satisfy most applications.

PCB Layout Recommendations

When laying out the printed circuit board, the following checking should be used to ensure proper operation of the JTM3420D. Check the following in your layout:

- The power traces, consisting of the GND trace, the SW trace and the VIN trace should be kept short, direct and wide
- Does the (+) plates of C_{IN} connect to VIN as closely as possible. This capacitor provides the AC current to the internal power MOSFETs.
- Keep the switching node, SW, away from the sensitive V_{OUT} node.
- Keep the (-) plates of C_{IN} and C_{OUT} as close as possible.

PACKAGE DESCRIPTION



NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
3. EXPOSED PAD SHALL BE SOLDER PLATED
4. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE