SYNCHRONOUS BOOST CONVERTER

With 5A Switch, Can Output 5V 2.5A with Li-Battery Input

GENERAL DESCRIPTION

JTM5178 is a high efficiency synchronous boost regulator that converts down to 2.5V input and up to 5.5V output voltage. It adopts NMOS for the main switch and PMOS for the synchronous switch. It can disconnect the output from input during the shutdown mode..

It integrates 5A power MOSFET and can output 5V 2.5A with Li-Battery input.

FEATURES

- 2.5V Minimum input voltage
- Adjustable output voltage from 3V to 5. 5V
- 6A peak current limit
- Input under voltage lockout
- 600Khz fixed Switching Frequency
- Load disconnect during shutdown
- Integrated soft-start
- Output over voltage protection
- 30moJTM Power MOSFET
- Thermal Shutdown
- QFN4x4-16 Package

APPLICATIONS

Handheld Devices

Power Bank

All Single Cell Li or Dual Cell Battery Operated Products

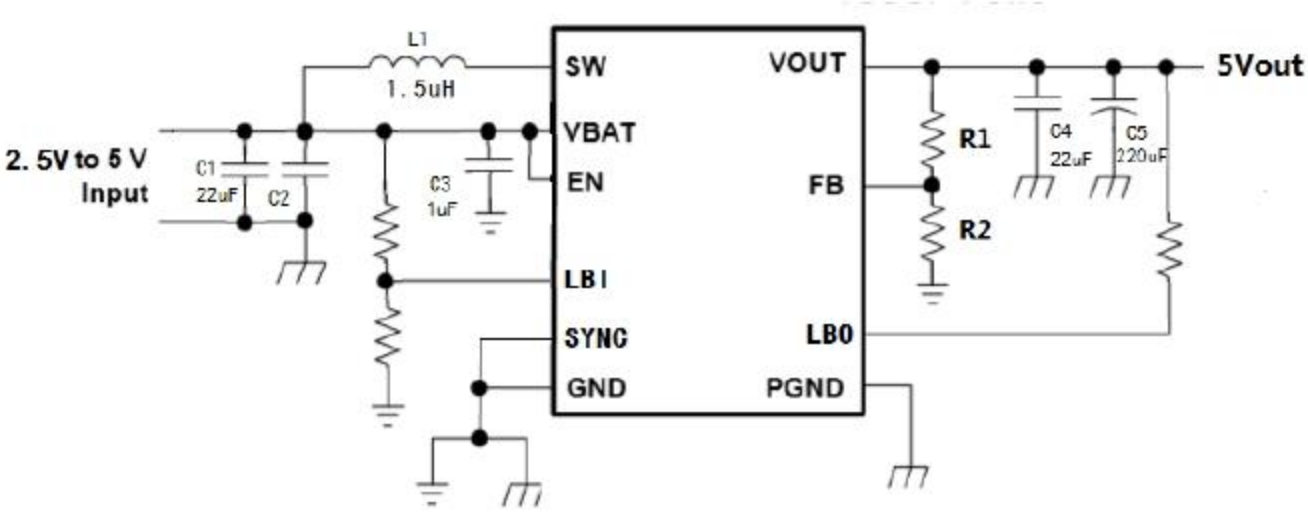


Figure 1. Typical Application Circuit

ORDERING INFORMATION

PART NUMBER	TEMP RANGE	SWICHING FREQUENCY	OUTPUT VOLTAGE (V)	ILIM (A)	PACKAGE	PINS
JTM5178	-40°C to 85°C	600KHZ	ADJ	>6	QFN4*4	16

PIN CONFIGURATION

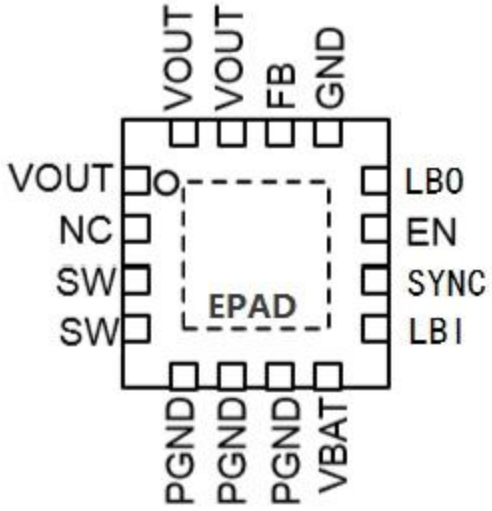


Figure 2. PIN Configuration

PIN DESCRIPTION

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1,15,16	Vout	DC-DC Boost output
3,4	SW	Switch pin , Connect an inductor between IN pin and LX pin.
5,6,7	PGND	Power ground
8	VBAT	VDD Power Supply，need one 1uF MLCC close to VBAT pin and AGND
9	LBI	Low battery comparator input (comparator enabled with EN)
10	SYNC	Enable/disable power save mode (1/VBAT disabled, 0/GND enabled)
11	EN	Shutdown control input., Connect this pin to logic high level to enable the device
12	LBO	Low battery comparator output (open drain)
13	GND	Analog ground
14	FB	Feedback pin
2	NC	No Connected
17	EPAD	Thermal pad, Should connect with Power ground

ABSOLUTE MAXIMUM RATINGS

(Note: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

PARAMETER	VALUE	UNIT
EN Voltage	Vout+0.3V	V
Other Pins	6V	V
Operating Ambient Temperature	-40 to 85	°C
Maximum Junction Temperature	150	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, T_A= 25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{IN}		2.5		5.5	V
Boost output voltage range	Vout		2.5		5.5	V
UVLO Threshold	V_{UVLO}	$V_{HYSTERESIS}$ =100mV		2.2		V
Operating Supply Current	I_{SUPPLY}	V_{FB} =1.3V， EN=Vin=3.6V, I_{Load} =0		85		µA
Shutdown Supply Current		V_{EN} =0V, V_{IN} =3.6V			1	
Regulated Feedback Voltage	V_{FB}		1.18	1.2	1.22	V
Peak inductor Current limit (N-MOSFET current limit)	Ilim		6			A
Oscillator Frequency	F_{OSC}			0.6		MHz
Rds(ON) of N-channel FET		I_{SW} =-100mA		30		mOJTM
*Enable Threshold		V_{IN} = 2.3V to 5.5V	0.3	1	1.5	V
Enable Leakage Current			-0.1		0.1	µA
SW Leakage Current		V_{EN} = 0V, V_{SW} = 0V or 5V, V_{IN} = 5V			1	uA
Output over voltage protection				6		V
Minimum on time				100		ns
Minimum off time				100		ns

Soft Start Time	Tss			1.5		ms
LBI voltage threshold		VLBI voltage decreasing		0.5		V

*Note: Please set EN voltage 〈Vbat voltage, the best EN voltage from MCU is 2V

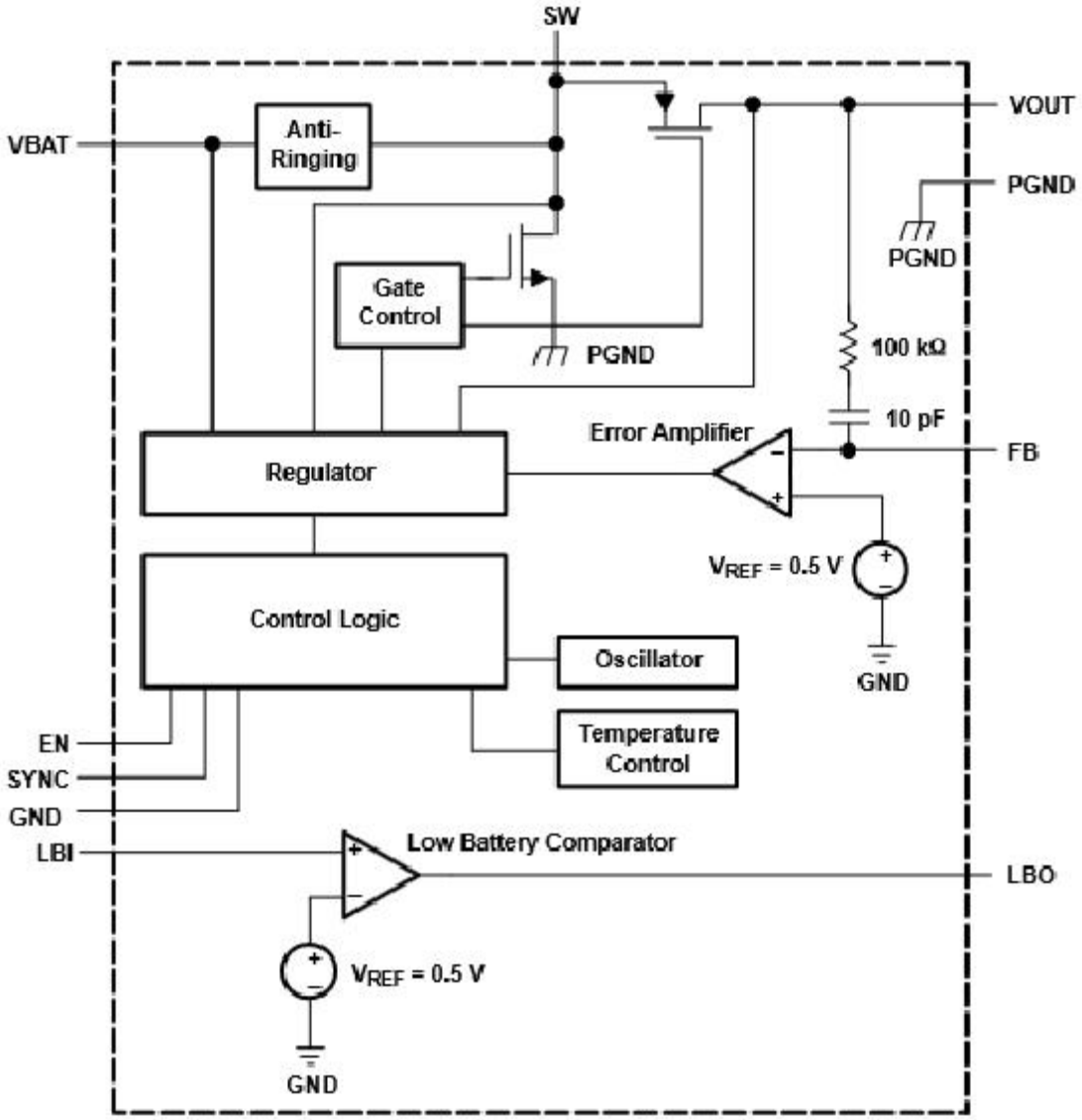


Figure 3. Functional Block Diagram

CONTROLLER CIRCUIT

The controller circuit of the device is based on a fixed frequency multiple feedforward controller topology. Input voltage, output voltage, and voltage drop on the NMOS switch are monitored and forwarded to the regulator. So changes in the operating conditions of the converter directly affect the duty cycle and must not take the indirect and slow way through

the control loop and the error amplifier. The control loop, determined by the error amplifier, only has to handle small signal errors. The input for it is the feedback voltage on the FB pin, the voltage on the internal resistor divider. It is compared with the internal reference voltage to generate an accurate and stable output voltage.

The peak current of the NMOS switch is also sensed to limit the maximum current flowing through the switch and the inductor. The typical peak current limit is set to exceed 6A. An internal temperature sensor prevents the device from getting overheated in case of excessive power dissipation.

SYNCHRONOUS RECTIFIER

The device integrates an N-channel and a P-channel MOSFET transistor to realize a synchronous rectifier. Because the commonly used discrete Schottky rectifier is replaced with a low RDS(ON) PMOS switch, the power conversion efficiency reaches 96%. To avoid ground shift due to the high currents in the NMOS switch, two separate ground pins are used. The reference for all control functions is the GND pin. The source of the NMOS switch is connected to PGND. Both grounds must be connected on the PCB at only one point close to the GND pin. A special circuit is applied to disconnect the load from the input during shutdown of the converter. In conventional synchronous rectifier circuits, the backgate diode of the high-side PMOS is forward biased in shutdown and allows current flowing from the battery to the output. This device however uses a special circuit which takes the cathode of the backgate diode of the high-side PMOS and disconnects it from the source when the regulator is not enabled (EN = low).

The benefit of this feature for the system design engineer is that the battery is not depleted during shutdown of the converter. No additional components have to be added to the design to make sure that the battery is disconnected from the output of the converter.

LOW BATTERY DETECTOR CIRCUIT—LBI/LBO

The low-battery detector circuit is typically used to supervise the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage. The function is active only when the device is enabled. When the device is disabled, the LBO pin is high-impedance. The switching threshold is 500 mV at LBI. During normal operation, LBO stays at high impedance when the voltage, applied at LBI, is above the threshold. It is active low when the voltage at LBI goes below 500 mV.

The battery voltage, at which the detection circuit switches, can be programmed with a resistive divider connected to the LBI pin. The resistive divider scales down the battery voltage to a voltage level of 500 mV, which is then compared to the LBI threshold voltage. The LBI pin has a built-in hysteresis of 10 mV. See the application section for more details about the programming of the LBI threshold. If the low-battery detection circuit is not used, the LBI pin should be connected to GND (or to VBAT) and the LBO pin can be left unconnected.

For this version, LBI/LBO function is error. Next version will be corrected.

OUTPUT VOLTAGE PROGRAMMING

In the adjustable version, the output voltage is set by a resistive divider according to the following equation:

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{1.2} - 1 \right)$$

Typically choose R2=100K and determine R1 from the following equation。

INDUCTOR SELECTION

In normal operation, the inductor maintains continuous current to the output. The inductor current has a ripple that is dependent on the inductance value. The high inductance reduces the ripple current. For power bank application,1uH~2.2uH is suitable.

SELECTED INDUCTOR BY ACTUAL APPLICATION:

Manufacturer	*Part Number*	*Inductance(uH)*	*DRC max (OJTMs*	*Dimensions L*W*H(mm3)*
Marata	LQH5BP	1.0	0.019	5*5*2
		1.5	0.024	
		2.2	0.030	
TDK	SPM6530T	1.0	0.007	7.1*6.5*3
		1.5	0.01	
		2.2	0.017	
		3.3	0.027	
WURTH	74437346010	1.0	0.008	7.3*6.6*2.8

Table 1. Recommend Surface Mount Inductors

INPUT CAPACITOR

One or Two 22μF MLCC capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. Two 22μF MLCC capacitor is recommended. One 1uF MLCC capacitor is needed close to Vbat。

OUTPUT CAPACITOR

For 5V 2A~2.5A load, one 22uF MLCC+220uF E-cap is minim and low ESR tantalum capacitor is recommended

LAYOUT CONSIDERATIONS

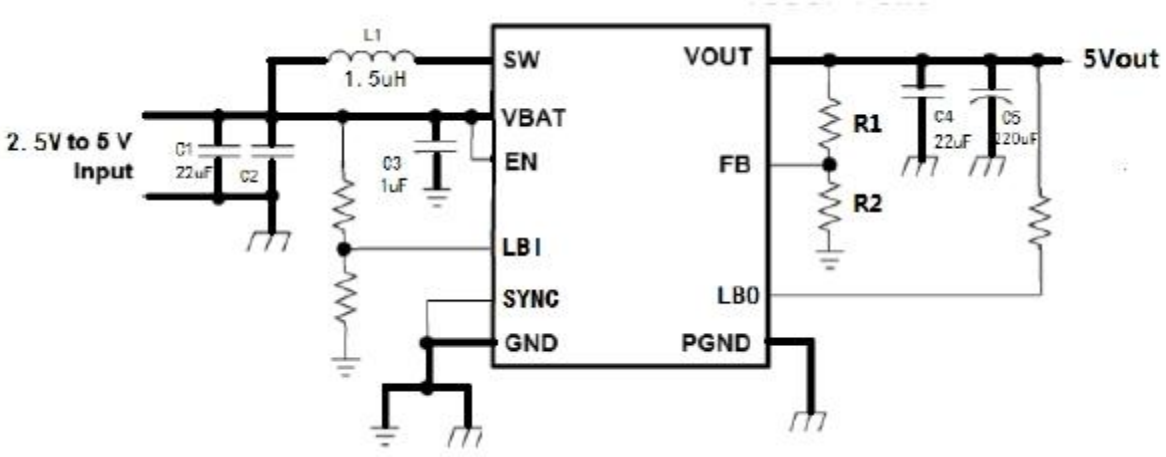
1：The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC.

2：Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise.

3：The feedback divider should be placed as close as possible to the control ground pin of the IC. The components R1 and R2, and the trace connecting to the FB pin must NOT be adjacent to the SW net on the PCB layout to avoid the noise problem

4：Please make sure that the big current circuits are board and short to reduce the circuit Rdson

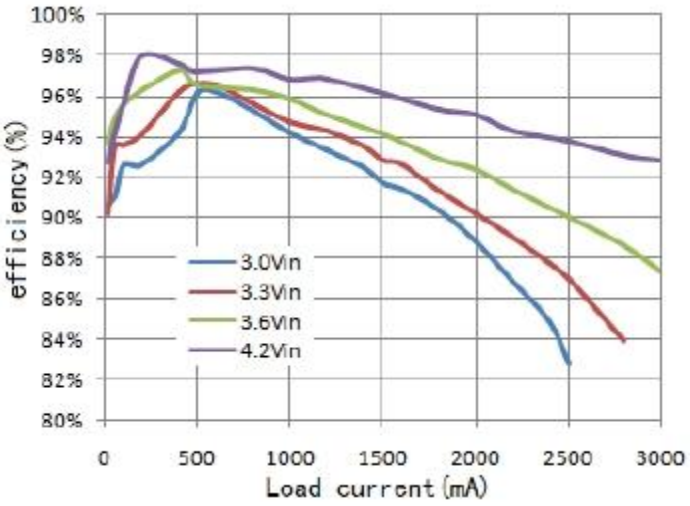
5：The big current path must be broad line in PCB just as below。Ibat may be big current at startup so it also need broad and short line. It is desirable to maximize the PCB copper area connecting to GND/EPAD pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable。



EFFICIENCY FIGURE

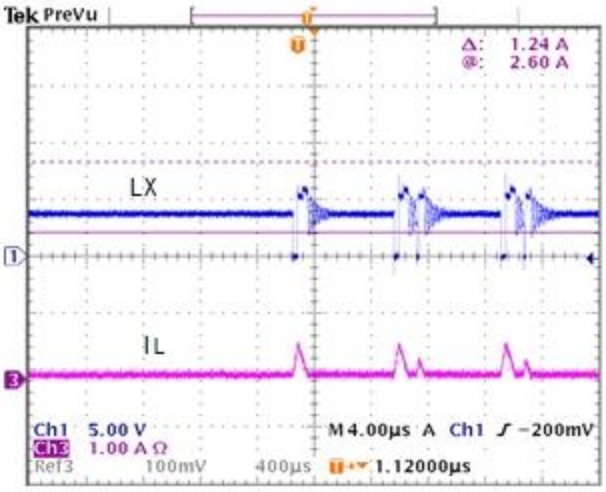
(L=2.2uH, CIN=22uF MLCC*2, COUT=22uF MLCC+220uF E-Cap,if not mentioned)

Efficiency Vs Load Current



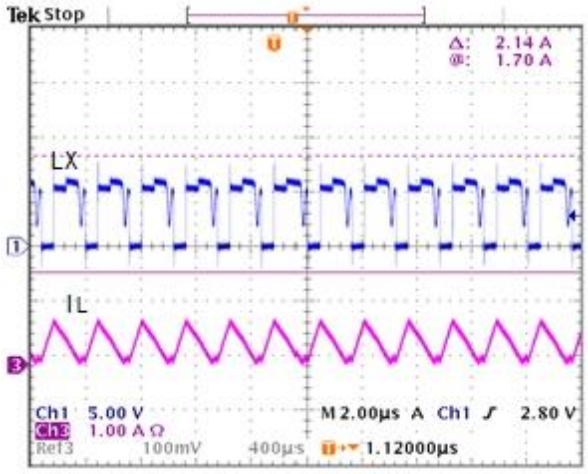
Steady State

(3.6Vin 5Vout Io=0A)



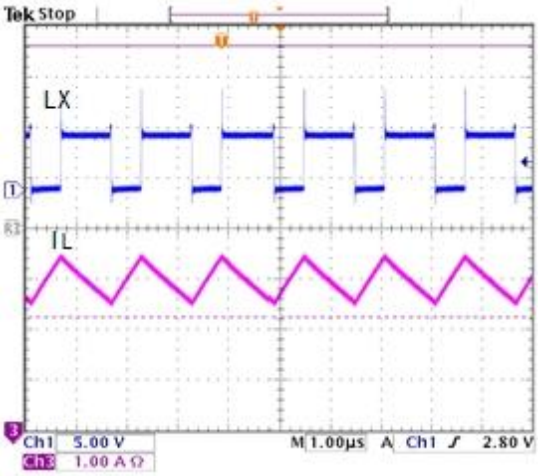
Steady State

(3.6Vin 5Vout Io=0.2A)



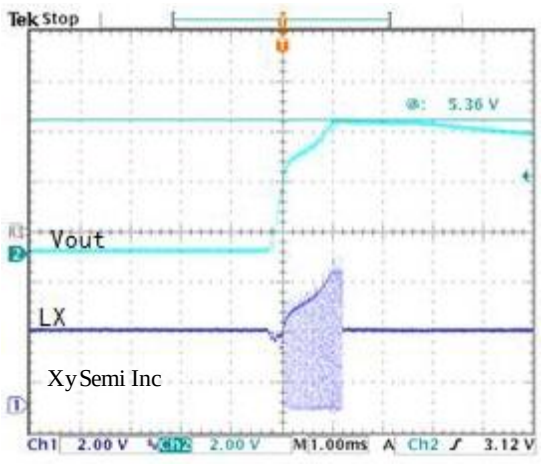
Steady State

(3.6Vin 5Vout Io=0.2A)



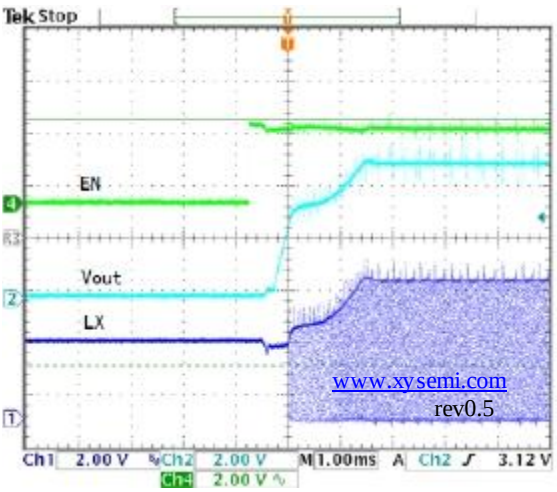
Startup from Vin

(EN、Vin from 0V to 3.6V)



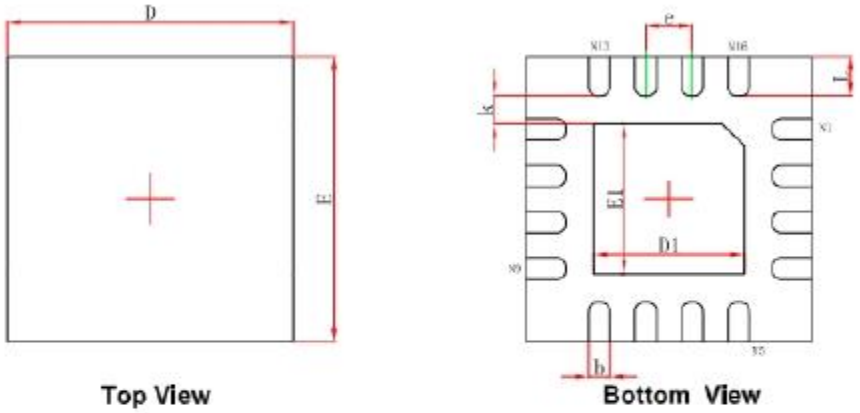
Startup from EN

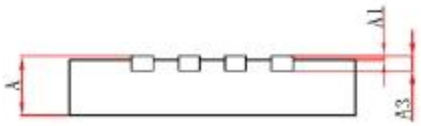
(Vin=3.6V EN from 0V to 3.6V)



PACKAGE OUTLINE

QFN4X4-16 PACKAGE OUTLINE AND DIMENSIONS





Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
D1	2.000	2.200	0.079	0.087
E1	2.000	2.200	0.079	0.087
k	0.200MIN.		0.008MIN.	
b	0.250	0.350	0.010	0.014
e	0.650TYP.		0.026TYP.	
L	0.450	0.650	0.018	0.026