3A, 28V, 1MHz Synchronous Step-Down Converter

DESCRIPTION

The EUP3475A is a 1MHz fixed frequency synchronous current mode buck regulator. The device integrates both 135mΩ high-side switch and 90mΩ low-side switch that provide 3A of continuous load current over a wide operating input voltage of 4.5V to 28V.The internal synchronous power switch increases efficiency and eliminates the need for an external Schottky diode. Current mode control provides fast transient response and cycle-by-cycle current limit.

At heavy load, the EUP3475A operates at a fixed frequency Pulse-Width Modulation mode for excellent stability and transient response. At light load, the EUP3475A will operates at a Pulse-Skipping mode to save power.

The EUP3475A features short circuit and thermal protection circuits to increase system reliability. Externally programmable soft-start allows for proper power on sequencing with respect to other power supllies and avoids input inrush current during startup. In shutdown mode, the supply current drops below 1μA. The EUP3475A is available in SOP-8 package with the exposed pad.

FEATURES

- Automatic Pulse Skipping Mode at Light Load
- 3A Continuous Output Current
- 110ns Minimum On Time
- Integrated 135mΩ High Side Switch
- Integrated 90mΩ Low Side Switch
- Wide 4.5V to 28V Operating Input Range
- Output Adjustable from 0.8V to 24V
- Up to 95% Efficiency
- Programmable Soft-Start
- <1μA Shutdown Current
- 1MHz Fixed Switching Frequency
- Thermal Shutdown and Over Current Protection
- Input Under Voltage Lockout
- Available in SOP-8 (EP) package
- RoHS Compliant and 100% Lead(Pb)-Free
- Halogen-Free

APPLICATIONS

- Distributed Power Systems
- Networking Systems
- FPGA, DSP, ASIC Power Supplies

Typical Application Circuit

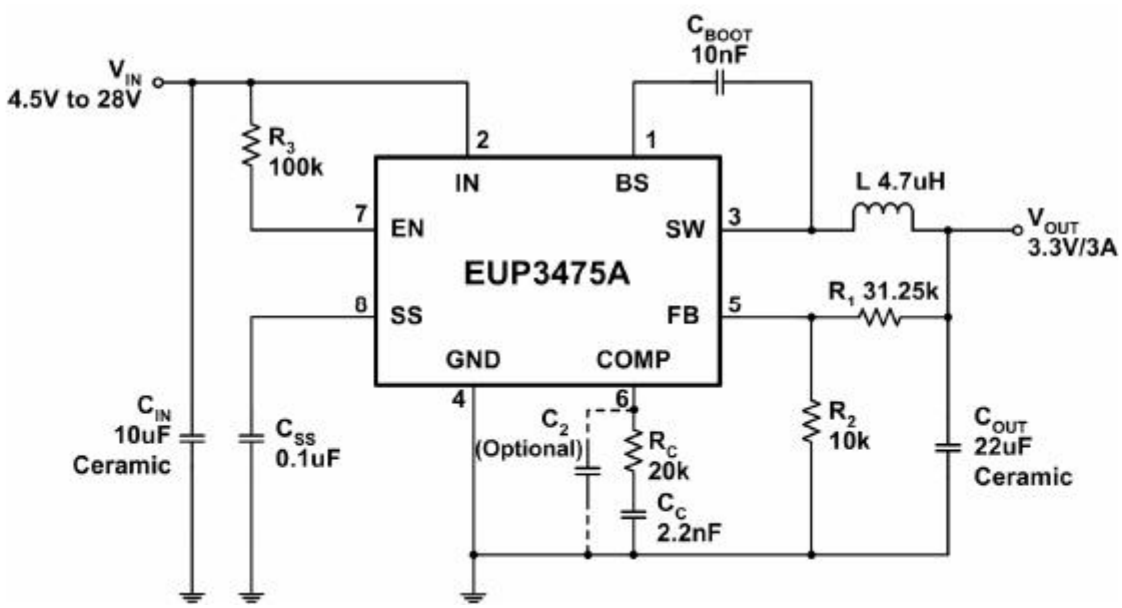
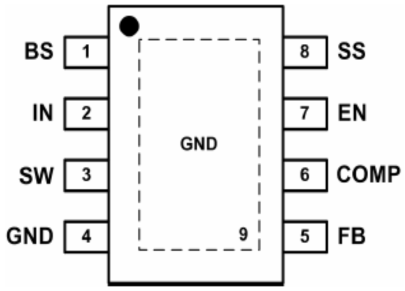


Figure 1.

Pin Configurations

Package Type	Pin Configurations
SOP-8 (EP)	

Pin Description

Number	Pin Name	Description
1	BS	High-Side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel DMOS switch. Connect a 0.01µF or greater capacitor from SW to BS to power the high side switch.
2	IN	Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.5V to 28V power source. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See *Input Capacitor*.
3	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.
4 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
5	FB	Feedback Input. FB senses the output voltage and regulates it. Drive FB with a resistive voltage divider connected to it from the output voltage. The feedback threshold is 0.8V. See *Setting the Output Voltage*.
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND. In some cases, an additional capacitor from COMP to GND is required. See *Compensation Components*.
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; low to turn it off. Connect to IN with a 100K pull up resistor for automatic startup.
8	SS	Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the external soft-start period, or leave SS floating to set the internal soft-start period. A 0.1µF capacitor sets the soft-start period to about 15ms. Leave SS pin floating, and the internal soft-start period is about 300µs.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUP3475ADIR1	SOP-8 (EP)	xxxxx 3475A	-40 ℃ to +85℃

EUP3475A □ □ □ □

- Lead Free Code
  1: Lead Free, Halogen Free 0: Lead
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  D: SOP

Block Diagram

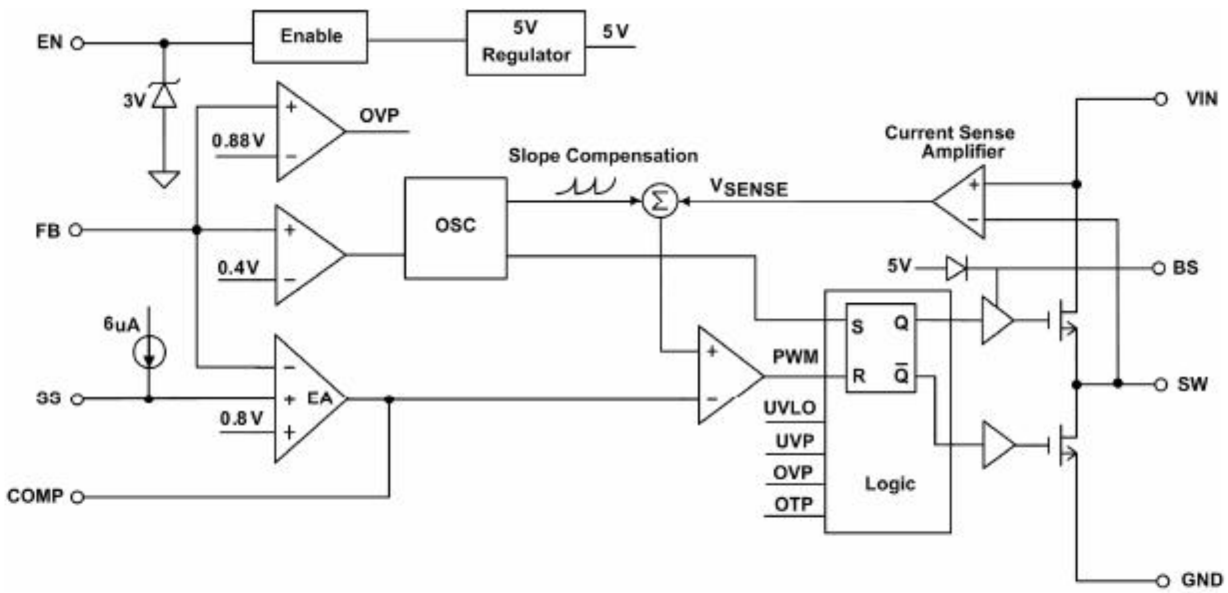


Figure 2. EUP3475A Functional Block Diagram

Absolute Maximum Ratings (1)

Supply Voltage (V_{IN}) -- -0.3V to +30V
EN Voltage (V_{EN}) -- -0.3V to +6V
Switch Voltages (V_{SW}) -- -1V to V_{IN} +0.3V
Bootstrap Voltage (V_{BS}) -- V_{SW} -0.3V to V_{SW} +6V
All Other Pins -- -0.3V to +6V
Junction Temperature --- 150 ℃
Lead Temperature -- 260 ℃
Storage Temperature -- -65 ℃ to 150 ℃
Output Voltage V_{OUT} --- 0.9V to 26V
Thermal Resistance
θ_{JA} (SOP-8_EP) --- 60 ℃ /W
ESD Ratings
Human Body Mode --- ±2kV

Recommend Operating Conditions (2)

Input Voltage (V_{IN}) -- 4.5V to 28V
Operating Temperature Range --- -40 ℃ to +85 ℃

Note (1): Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.
Note (2): The device is not guaranteed to function outside the recommended operating conditions.

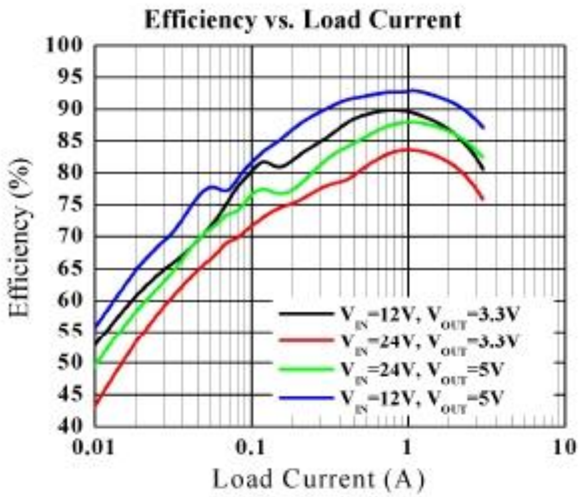
Electrical Characteristics

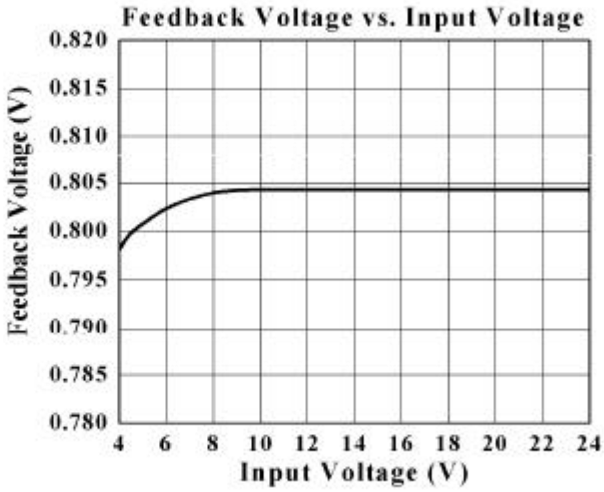
Unless otherwise specified, V_{IN}=12V ,T_A=+25 ℃.

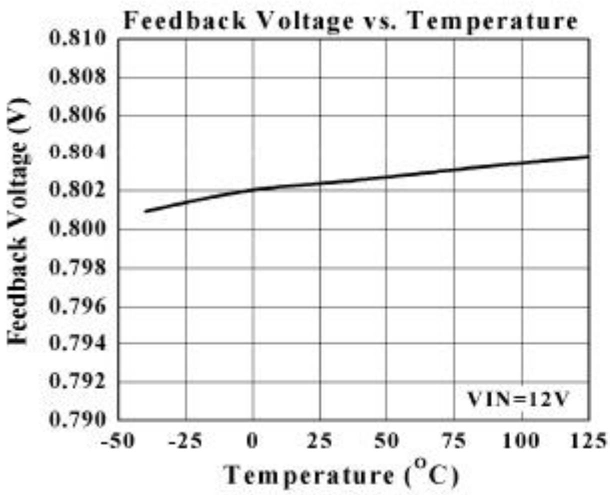
Symbol	Parameter	Conditions	EUP3475A			Unit
			Min	Typ	Max.	
I_{SHUT}	Shutdown Supply Current	V_{EN}=0V		0.1	3	μA
I_Q	Supply Current	V_{EN}=2V, V_{COMP}=0.35V		1.1	1.5	mA
V_{FB}	Feedback Voltage	4.5V≦V_{IN}≦28V	0.784	0.800	0.816	V
A_{EA}	Error Amplifier Voltage Gain			400		V/V
G_{EA}	Error Amplifier Transconductance	ΔI_C = ±10μA		400		μA/V
$R_{DS(ON)\,1}$	High-Side Switch On-Resistance	I_{SW}=300mA		135		mΩ
$R_{DS(ON)\,2}$	Low-Side Switch On-Resistance	I_{SW}=300mA		90		
$I_{LEAKAGE}$	High-Side Switch Leakage Current	V_{EN}=0V, V_{SW}=0V		0	10	μA
I_{LIMIT}	Upper Switch Current Limit	Minimum Duty Cycle	3.6	4.8		A
I_{NEG}	Low-side Switch Reverse Current Limit	From Drain to Source		0		
G_{CS}	COMP to Current Sense Transconductance			5.6		A/V
F_{OSC1}	Oscillation Frequency	V_{FB}=0.76V	0.8	1	1.2	MHz
F_{OSC2}	Short Circuit Oscillation Frequency	V_{FB}=0V		200		KHz
D_{MAX}	Maximum Duty Cycle	V_{FB}=0.76V		90		%
T_{ON}	Minimum On Time			110		ns
V_{EN}	EN Shutdown Threshold Voltage	V_{EN} Rising	1.1	1.5	2	V
V_{EHHYS}	EN Shutdown Threshold Voltage Hysterisis			0.2		
V_{UVLO}	Input Under Voltage Lockout Threshold	V_{IN} Rising	3.8	4.0	4.2	
$V_{UVLOHYS}$	Input Under Voltage Lockout Threshold Hysteresis			0.2		
I_{SS}	Soft-Start Current	V_{SS}=0V		6		μA
T_{SS}	Soft-Start Period	C_{SS}=0.1μF		15		ms
T_{SD}	Thermal Shutdown			160		℃
T_{SDHYS}	Thermal Shutdown Hysteresis			20		

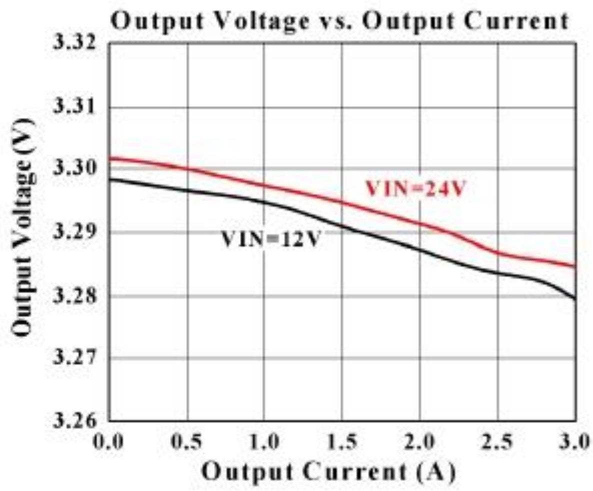
Typical Operating Characteristics

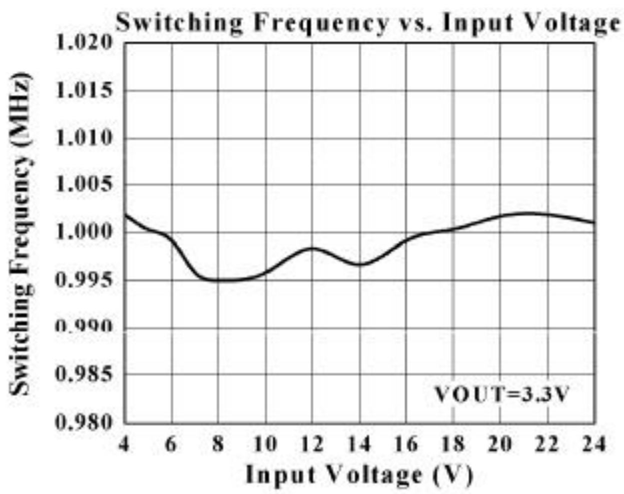
(C_{IN}=10μF, C_{OUT}= 2 · 10μF, L=4.7μH, C_{SS}=0.1μF ,T_A=+25℃, unless otherwise noted.)

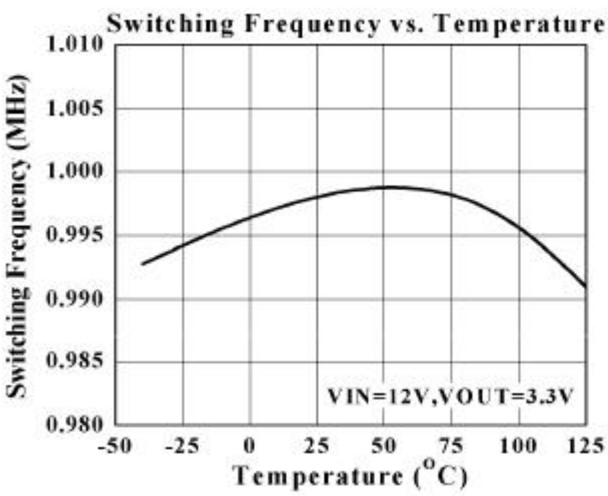






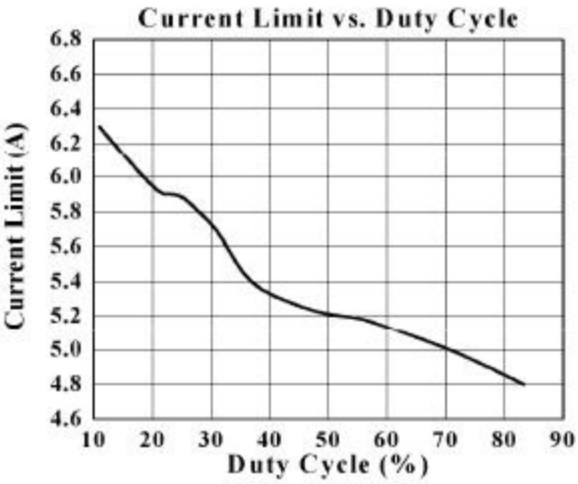


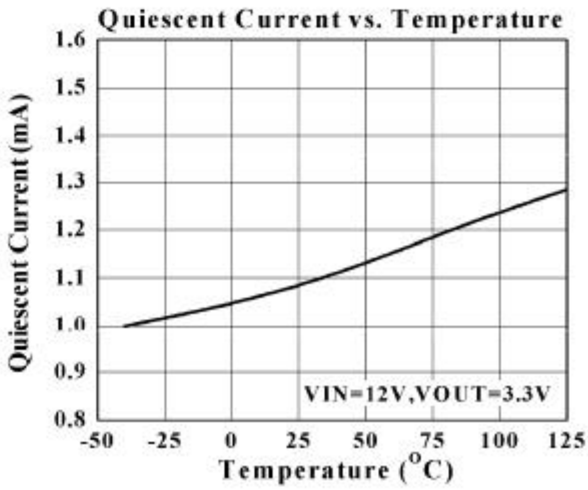


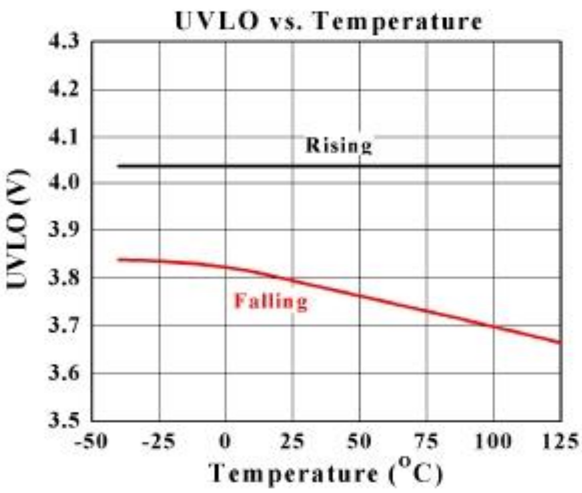


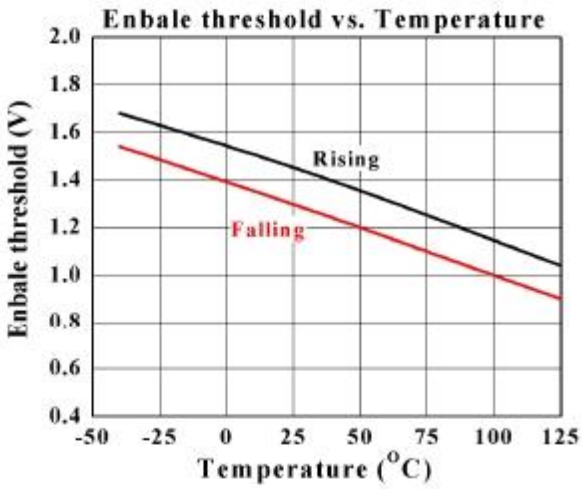
Typical Operating Characteristics (Continued)

(C_{IN}=10μF, C_{OUT}= 2 · 10μF, L=4.7μH, C_{SS}=0.1μF ,T_A=+25℃, unless otherwise noted.)

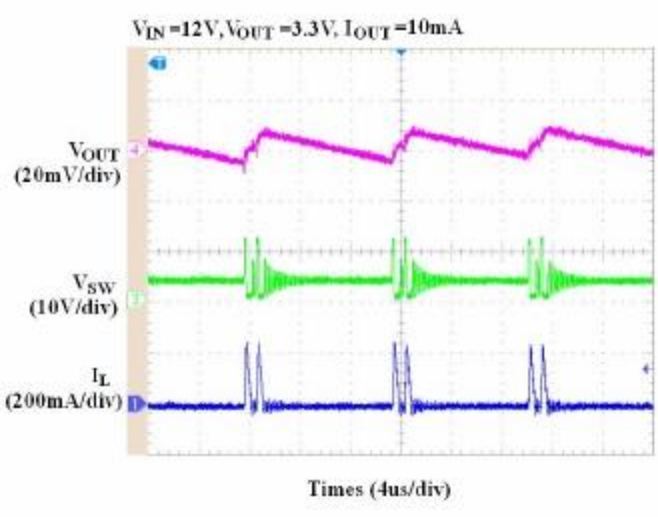




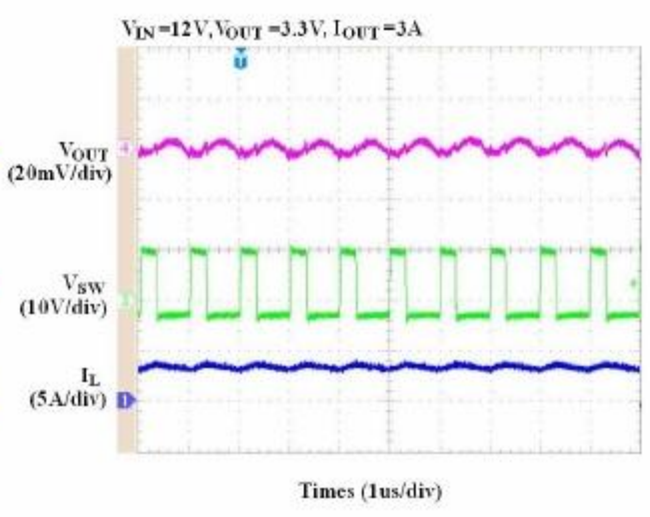




Output Ripple



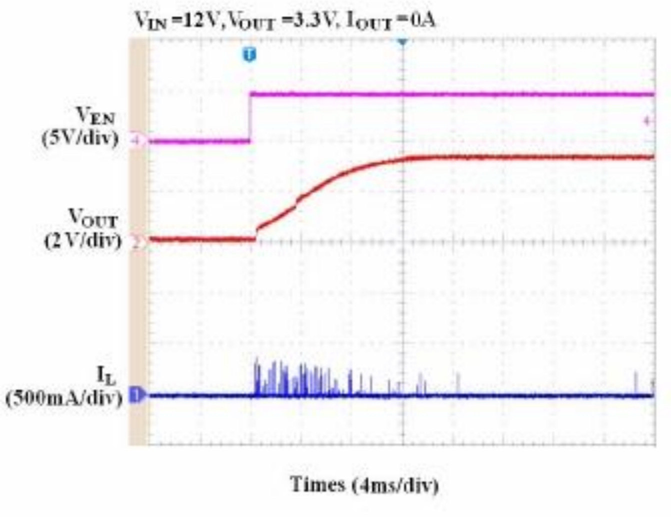
Output Ripple



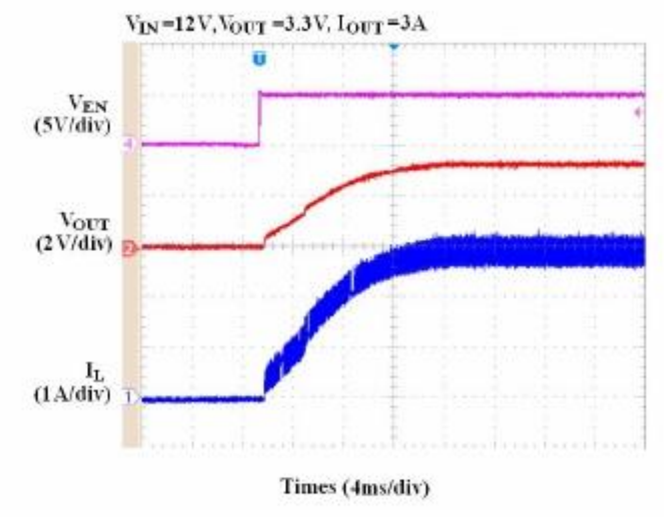
Typical Operating Characteristics (Continued)

(C_{IN}=10μF, C_{OUT}= 2 · 10μF, L=4.7μH, C_{SS}=0.1μF ,T_A=+25℃, unless otherwise noted.)

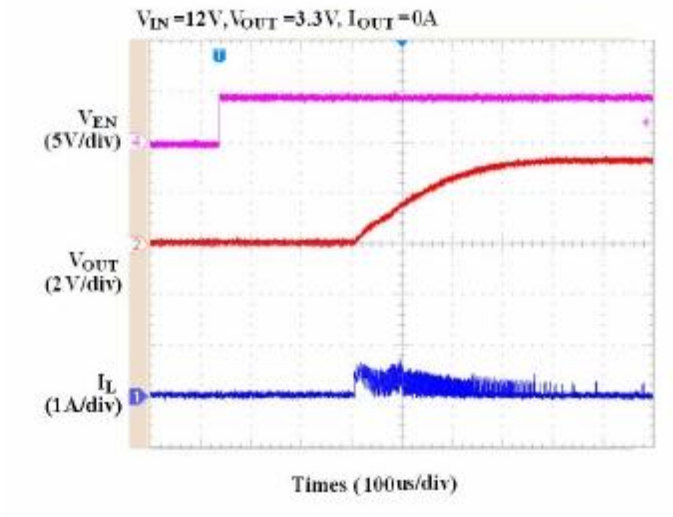
External Soft-Start



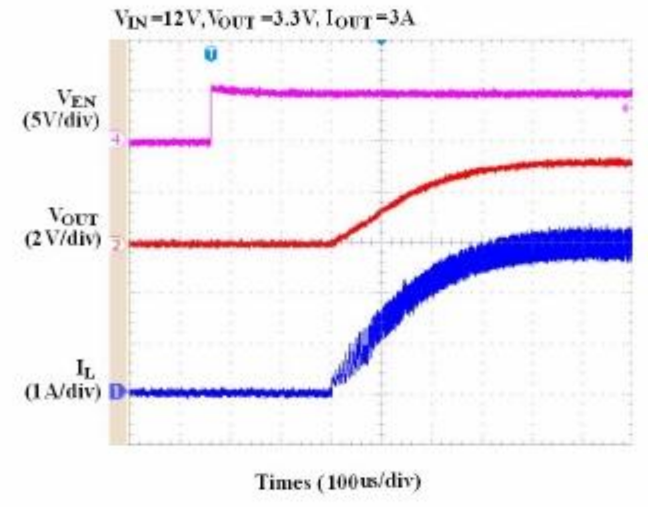
External Soft-Start



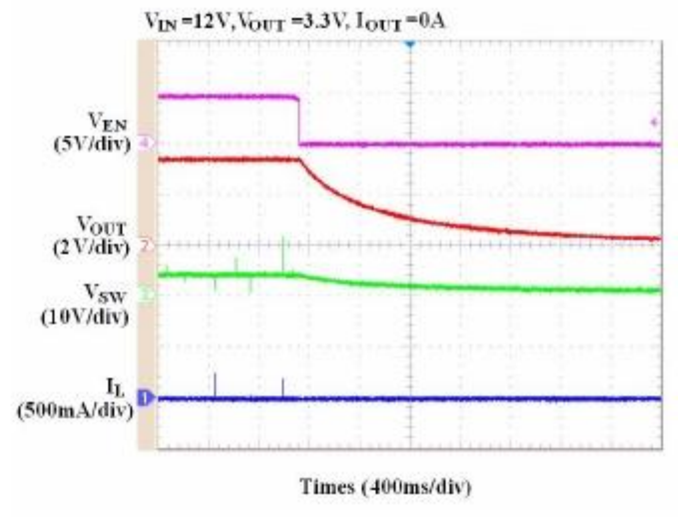
Internal Soft-Start (without Css Capacitor)



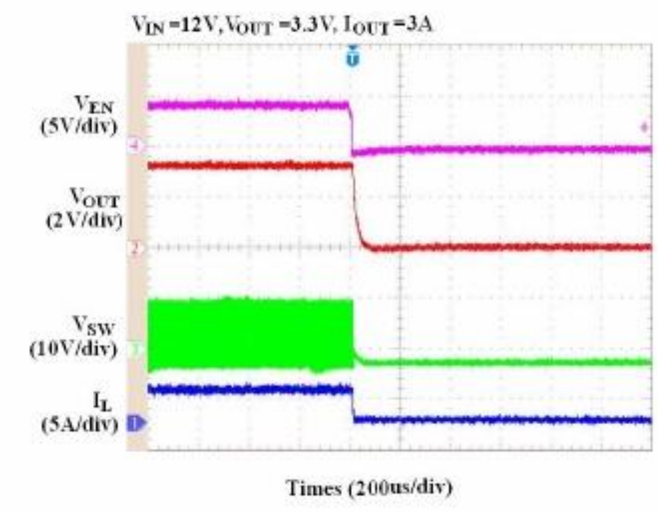
Internal Soft-Start (without Css Capacitor)



Shut Down



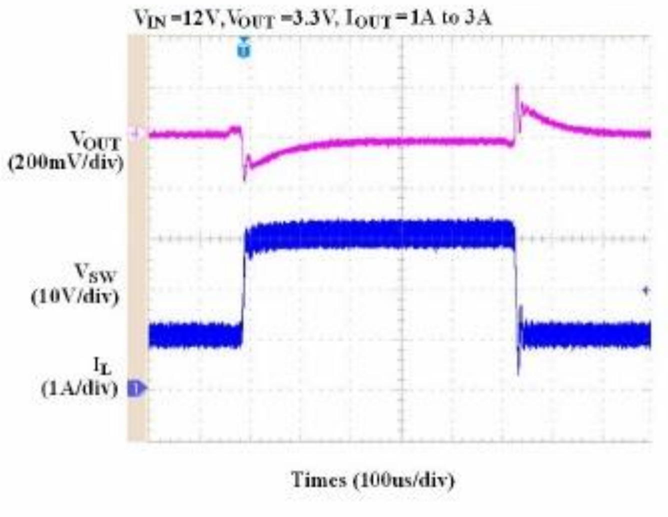
Shut Down



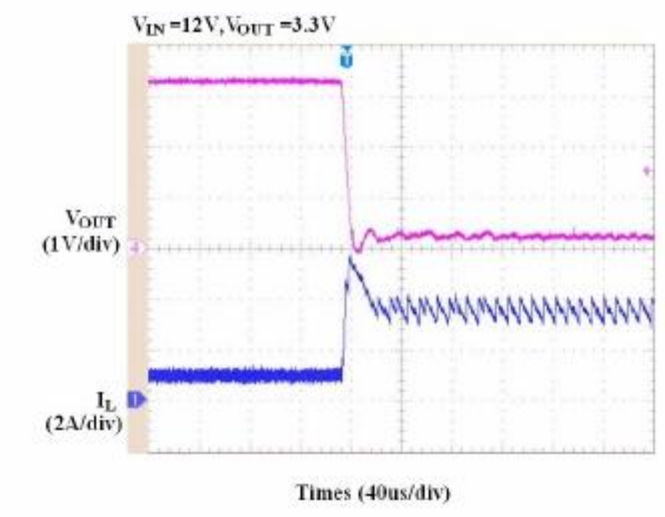
Typical Operating Characteristics (Continued)

(C_{IN}=10μF, C_{OUT}= 2 · 10μF, L=4.7μH, C_{SS}=0.1μF ,T_A=+25℃, unless otherwise noted.)

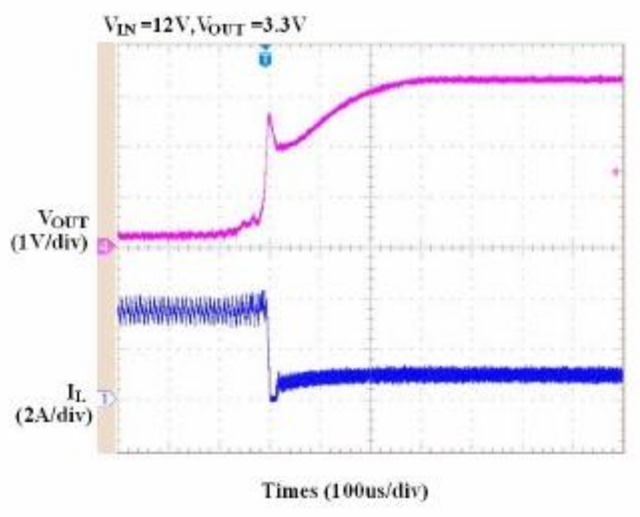
Load Transient Response



Short Circuit



Short Circuit Recovery



Application Information

Setting the Output Voltage

The output voltage is set using a resistive voltage divider connected from the output voltage to V_{FB}. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \cdot \frac{R_2}{R_1 + R_2}$$

Thus the output voltage is:

$$V_{OUT} = 0.8V \cdot \frac{R_1 + R_2}{R_2}$$

R_2 can be as high as 100kΩ, but a typical value is 10kΩ. Using the typical value for R_2, R_1 is determined by:

$$R_1 = (V_{OUT} - 0.8V) \cdot 12.5K$$

For example, for a 3.3V output voltage, R_2 is 10kΩ and R_1 is 31.25kΩ.

Inductor

The inductor is required to supply constant current to the load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will in turn results in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining inductance is to allow the peak-to-peak ripple current to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit.
The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S \cdot \Delta I_L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.
Choose an inductor that will not saturate under the maximum inductor peak current, calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \cdot f_S \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where I_{LOAD} is the load current.
The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI constraints.

Optional Schottky Diode

During the transition between the high-side switch and low-side switch, the body diode of the low-side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional Schottky diode may be paralleled between the SW pin and GND pin to improve overall efficiency.

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors will also suffice. Choose X5R or X7R dielectrics when using ceramic capacitors. Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{CIN} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where $I_{CIN} = I_{LOAD}/2$. For simplification, use an input capacitor with a RMS current rating greater than half of the maximum load current.
The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple for low ESR capacitors can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{C_{IN} \cdot f_S} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where C_{IN} is the input capacitor value. For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

Output Capacitor

The output capacitor (C_{OUT}) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot \left(R_{ESR} + \frac{1}{8 \cdot f_S \cdot C_{OUT}}\right)$$

Where C_{OUT} is the output capacitance value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.
When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance which is the main cause for the output voltage ripple. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \cdot f_S^2 \cdot L \cdot C_{OUT}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The EUP3475A can be optimized for a wide range of capacitance and ESR values.

Compensation Components

EUP3475A employs current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero combination to govern the characteristics of the control system. The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_{LOAD} \cdot G_{CS} \cdot A_{VEA} \cdot \frac{V_{FB}}{V_{OUT}}$$

Where V_{FB} is the feedback voltage (0.8V), A_{VEA} is the error amplifier voltage gain, G_{CS} is the current sense transconductance and R_{LOAD} is the load resistor value. The system has two poles of importance. One is due to the compensation capacitor (C_C) and the output resistor of the error amplifier, and the other is due to the output capacitor and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi \cdot C_C \cdot A_{VEA}}$$

$$f_{P2} = \frac{1}{2\pi \cdot C_{OUT} \cdot R_{LOAD}}$$

where G_{EA} is the error amplifier transconductance. The system has one zero of importance, due to the compensation capacitor (C_C) and the compensation resistor (R_C). This zero is located at:

$$f_{Z1} = \frac{1}{2\pi \cdot C_C \cdot R_C}$$

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$f_{ESR} = \frac{1}{2\pi \cdot C_{OUT} \cdot R_{ESR}}$$

In this case, a third pole set by the compensation capacitor (C_2) and the compensation resistor (R_C) is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

$$f_{P3} = \frac{1}{2\pi \cdot C_2 \cdot R_C}$$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause the system instability. A good standard is to set the crossover frequency below one-tenth of the switching frequency.

To optimize the compensation components, the following procedure can be used:

1. Choose the compensation resistor (R_C) to set the desired crossover frequency. Determine R_C by the following equation:

$$R_C = \frac{2\pi \cdot C_{OUT} \cdot f_C}{G_{EA} \cdot G_{CS}} \cdot \frac{V_{OUT}}{V_{FB}} < \frac{2\pi \cdot C_{OUT} \cdot 0.1 \cdot f_S}{G_{EA} \cdot G_{CS}} \cdot \frac{V_{OUT}}{V_{FB}}$$

Where f_C is the desired crossover frequency, which is typically below one tenth of the switching frequency.

2. Choose the compensation capacitor (C_C) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero (f_{Z1}) below one-forth of the crossover frequency provides sufficient phase margin. Determine C_C by the following equation:

$$C_C > \frac{4}{2\pi \cdot R_C \cdot f_C}$$

where R_C is the compensation resistor.

3. Determine if the second compensation capacitor (C_2) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency, or the following relationship is valid:

$$\frac{1}{2\pi \cdot C_{OUT} \cdot R_{ESR}} < \frac{f_S}{2}$$

If this is the case, then add the second compensation capacitor (C_2) to set the pole f_{P3} at the location of the ESR zero. Determine C_2 by the equation:

$$C_2 = \frac{C_{OUT} \cdot R_{ESR}}{R_C}$$

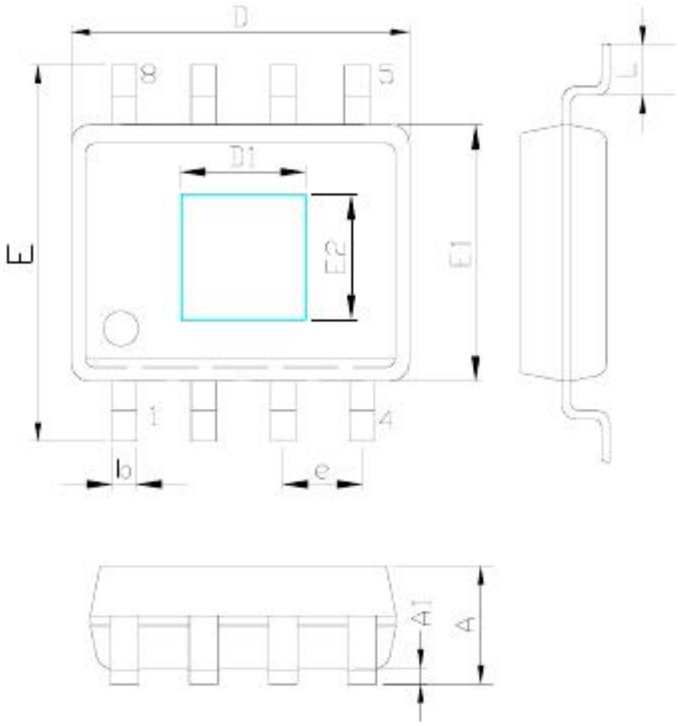
Table 1. Recommended Component Selection

（4.5V≤V_{IN}<28V）

V_{OUT}(V)	R_1(kΩ)	R_2(kΩ)	R_C(kΩ)	C_C(nF)	C_{OUT}(µF)	L(µH)
1.2V	5	10	10	2.2	22	2.2
1.5V	8.75	10	10	2.2	22	2.2
1.8V	12.5	10	13	2.2	22	2.2
2.5V	21.25	10	20	2.2	22	4.7
3.3V	31.25	10	20	2.2	22	4.7
5V	52.5	10	30	2.2	22	6.8
8V	90	10	41	2.2	22	6.8
10V	115	10	41	2.2	22	10
15V	177.5	10	60	2.2	22	10

Packaging Information

SOP-8 (EP)



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.90		0.193	
E1	3.90		0.153	
D1	2.00		0.081	
E2	2.00		0.081	
E	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
b	0.31	0.51	0.012	0.020
e	1.27		0.050	