Sensor-less 3A CC/CV Step-Down Converter

FEATURES

- 10V to 36V Input Voltage
- 40V Transparent Input Voltage Surge
- Up to 3A Constant Output Current
- Output Voltage Up to 15V
- High efficiency: up to 92%
- 225KHz Switching Frequency Eases EMI Design
- Integrated Sensor-less Constant Current (CC) Control
- Resistor Programmable for Current Limit from 1.5A to 3A
- ±8% CC Accuracy
- ±2% Feedback Voltage Accuracy
- Advanced Features Include
  - Integrated Soft-Start
  - Thermal Shut-down
  - Secondary Cycle-by-Cycle Current Limit
  - Protection Against Shorted ISET pin
- 8-lead SOP-EP Package

APPLICATIONS

- Car Charger/Adaptor
- Rechargeable Portable Devices
- General-Purpose CC/CV Supply

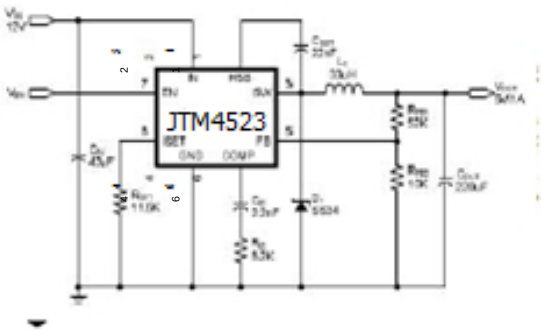
GENERAL DESCRIPTION

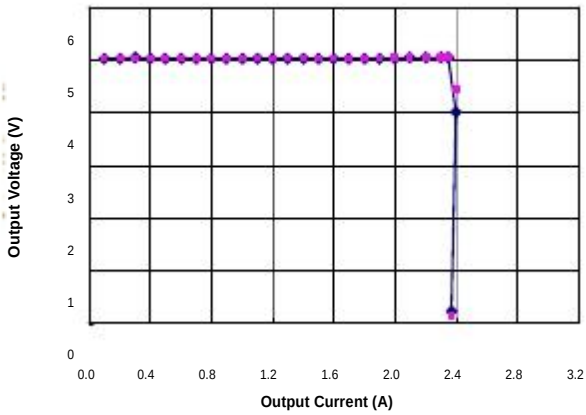
The JTM4523 is a wide input voltage high-efficiency Step-down DC/DC converter that operates in either CV (Constant Output Voltage) mode or CC (Constant Output Current) mode. JTM4523 provides up to 3A output current at 225-KHz switching frequency eases EMI design.

Integrated sensor-less CC control scheme of the JTM4523 eliminates the expensive, high accuracy current sense resistor, making it ideal for battery charging applications and adaptors with accurate current limit. The JTM4523 achieves higher efficiency than traditional constant current switching regulators by eliminating its associated power loss.

Protection features include cycle-by-cycle current limit, thermal shut-down, and frequency foldback at shot circuit. The devices are available in a SOP-8EP package and require very few external devices for operation.

TYPICAL APPLICATION

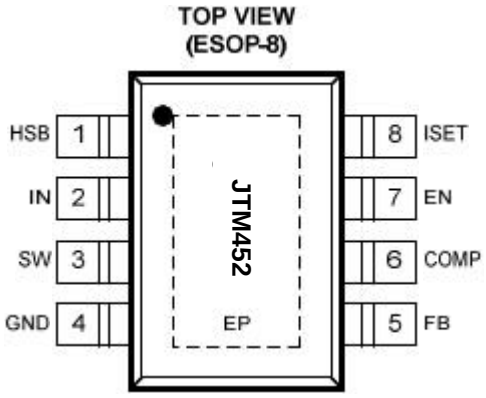




ORDER INFORMATION

Part Number	Current Limit	Temp Range	Package	Packing
JTM4523	3A	-40°C to +85°C	SOP-8EP	TAPE&REEL

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	PIN DESCRIPTION
1	HSB	High Side Bias Pin. This provides power to the internal high-side MOSFET gate driver. Connect a 22nF capacitor from BS pin to SW pin.
2	IN	Power Supply Input. Bypass this pin with a 10 F ceramic capacitor to GND, placed as close to the IC as possible.
3	SW	Power Switching Output to External Inductor.
4	GND	Ground. Connect this pin to a large PCB copper area for best heat dissipation. Return FB, COMP, and ISET to this GND, and connect this GND to power GND at a single point for best noise immunity.
5	FB	Feedback Input. The voltage at this pin is regulated to 0.8V. Connect to the resistor divider between output and GND to set the output voltage.
6	COMP	Error Amplifier Output. This pin is used to compensate the converter.
7	EN	Enable Input. EN is pulled up to 4.8V with a 10μA current, and contains a precise 1.6V logic threshold. Drive this pin to a logic-high or leave unconnected to enable the IC. Drive to a logic-low to disable the IC and enter shutdown mode.
8	ISET	Output Current Setting Pin. Connect a resistor from ISET to GND to program the output current.
	Exposed PAD	Heat Dissipation Pad. Connect this exposed pad to large ground copper area with copper and vias.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)

Input voltage range V_{IN}	V_{GND} 0.3V to V_{GND} 40V
SW pin voltage	V_{GND} 1.0V to V_{IN} 1.0V
HSB pin voltage	V_{SW} 0.3V to V_{SW} 7.0V
FB, EN, ISET, COMP to GND	V_{GND} 0.3V to V_{GND} 6V
ESOP8 Package thermal resistance	46°C/W
ESD Rating (Human Body Model (HBM))	2kV
Operating free-air temperature range, T_A	40°C to +150°C
Storage temperature range, T_{STG}	55°C to +150°C
Lead temperature(soldering, 10s), $T_{SOLDER1}$	+300°C

Note 1: Human Body Model (HBM) to Specification MIL-STD-883 Method 3015.7

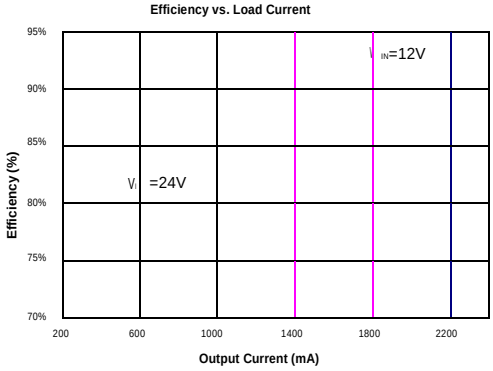
Note 2: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

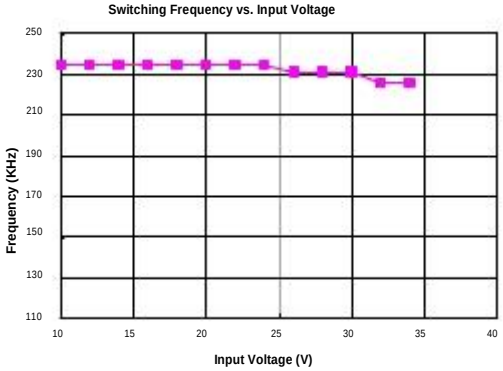
ELECTRICAL CHARACTERISTICS

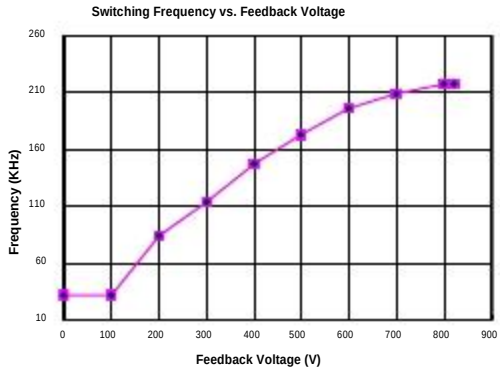
Typical values are at V_{IN}=20V, T_A = +25°C, unless otherwise specified

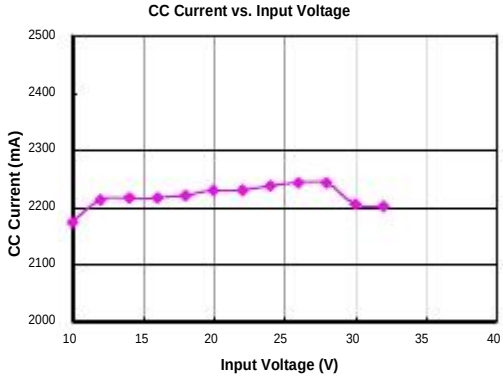
Parameter	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input voltage Range		10		40	V
Supply current	V_{EN}=3V,V_{FB}=1V,no switching		1.16		mA
	V_{EN}=3V,V_{OUT}=5V,No load		2.84		mA
Shutdown current	V_{EN}=0V		75	115	μA
Under voltage lockout Threshold	V_{IN} rising	9.0	9.1	9.3	V
Under voltage lockout Hysteresis			1.03		V
FB feedback voltage		796	811	830	mV
Internal soft-start time			600		us
Error amplifier Trans-conductance	V_{FB}=V_{COMP}=0.8V, I_{COMP}= 10 A		650		uA/V
Error amplifier DC gain			4000		V/V
Switching Frequency	V_{FB}=0.800V	215	230	240	kHz
Foldback switching frequency	V_{FB}=0V		30		kHz
Maximum Duty Cycle		85	88	91	%
Minimum On-Time			400		ns
COMP to current limit Trans-conductance	V_{COMP}=1.2V		5.25		A/V
Secondary cycle-by-cycle current limit	Duty=0%		4.5		A
Slope compensation	Duty=D_{MAX}		1.2		A
ISET voltage			1		V
ISET to IOUT DC current gain at room temperature	IOUT/ISET, R_{ISET}=19.6k		25000		A/A
CC controller DC accuracy	R_{ISET}=19.6k , V_{OUT}=3.5V Open-Loop DC Test	1175	1190	1205	mA
EN threshold voltage	EN Pin Rising	1.48	1.61	1.70	V
EN hysteresis voltage	EN Pin Falling		135		mV
EN internal Pull-up current			10		uA
High-Side switch ON-Resistance			0.16		
SW off leakage current	V_{EN}=V_{SW}=0V		1	6	uA
Thermal shutdown Temperature			150		°C
Thermal shutdown Hysteresis			20		°C

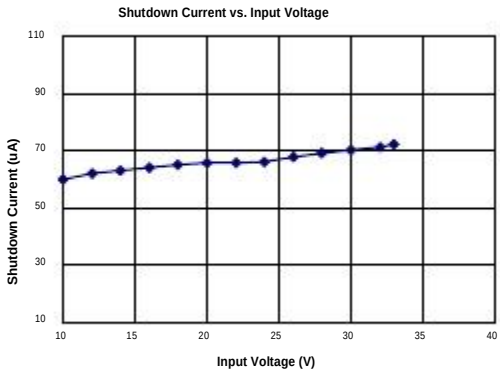
TYPICAL PERFORMANCE CHARACTERISTICS

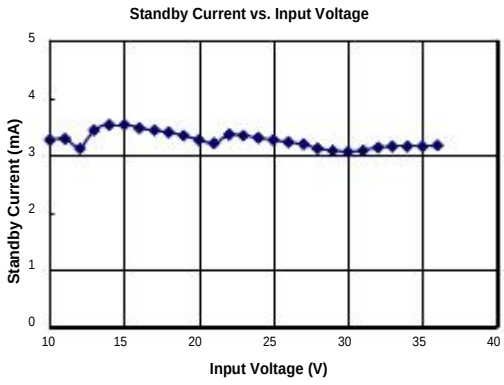






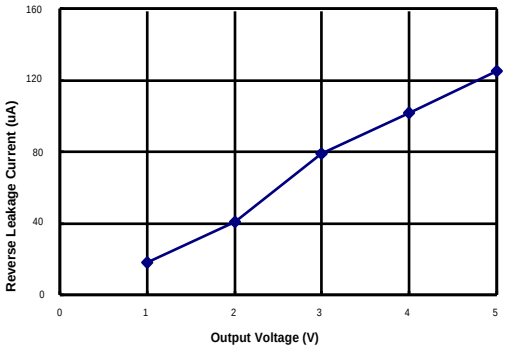




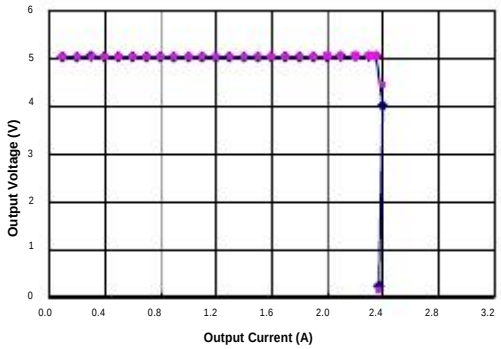


TYPICAL PERFORMANCE CHARACTERISTICS

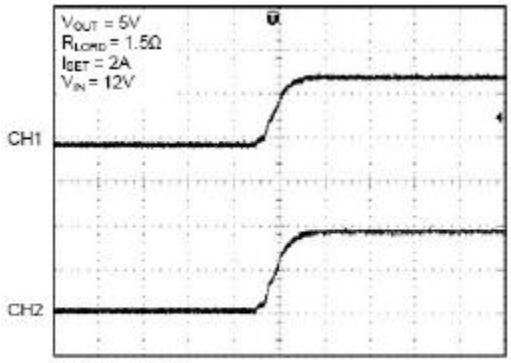
Reverse Leakage Current (IN pin Floating)



CC/CV Curver

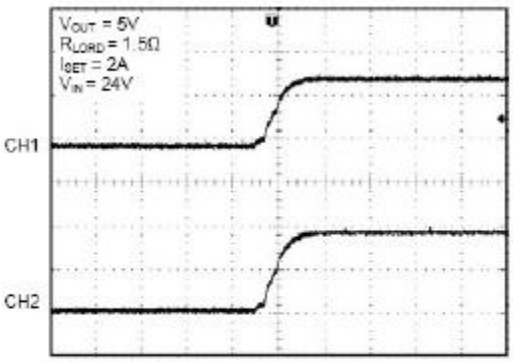


Startup into CC mode



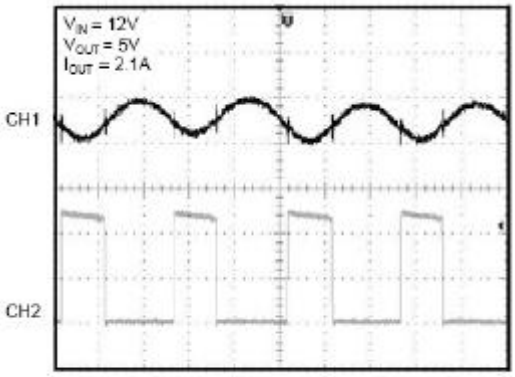
CH1: V_{OUT}, 2V/div
CH2: I_{OUT}, 1A/div
TIME: 200μs/div

Startup into CC mode



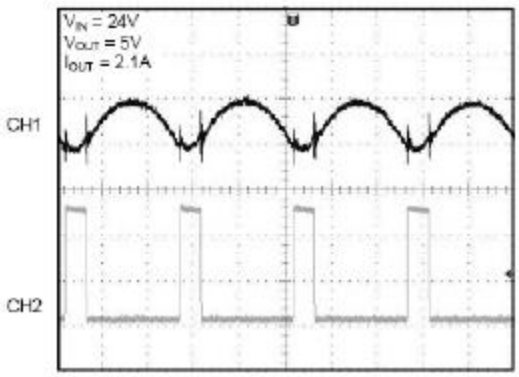
CH1: V_{OUT}, 2V/div
CH2: I_{OUT}, 1A/div
TIME: 200μs/div

SW vs. Output Ripple Voltage



CH1: V_{OUT} Ripple, 20mV/div
CH2: SW, 5V/div
TIME: 2μs/div

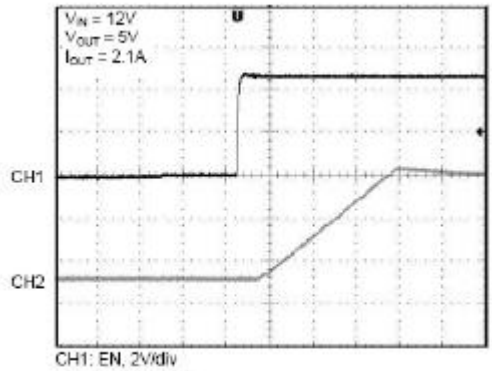
SW vs. Output Ripple Voltage



CH1: V_{RIPPLE}, 20mV/div
CH2: SW, 10V/div
TIME: 2μs/div

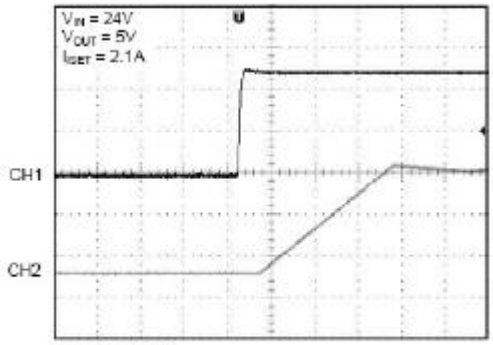
TYPICAL PERFORMANCE CHARACTERISTICS

Startup with EN



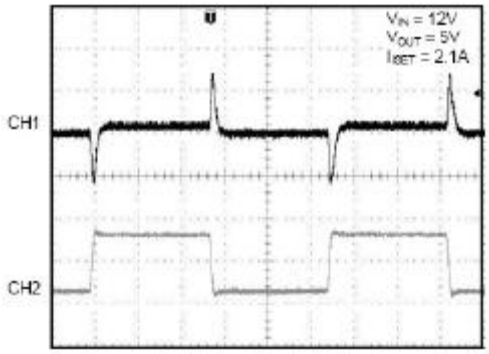
CH1: EN, 2V/div
CH2: V_{OUT}, 2V/div
TIME: 400μs/div

Startup with EN



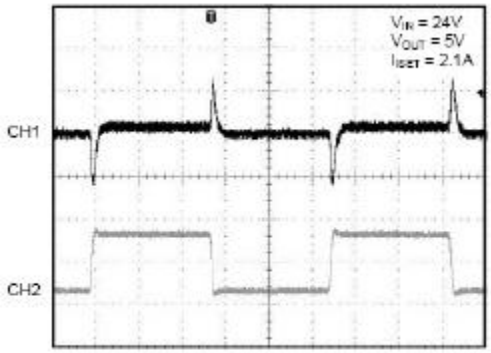
CH1: EN, 2V/div
CH2: V_{OUT}, 2V/div
TIME: 400μs/div

Load Regulation Waveform



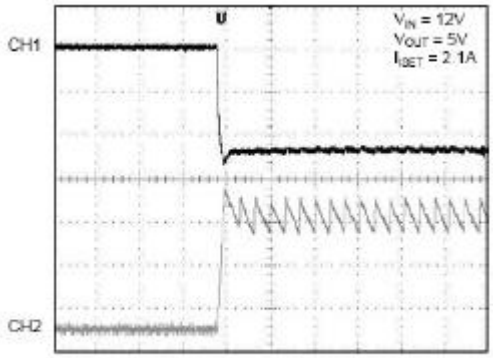
CH1: V_{OUT}, 200mV/div
CH2: I_{OUT}, 1A/div
TIME: 200μs/div

Load Regulation Waveform



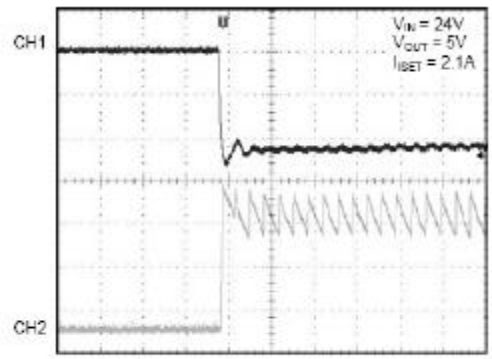
CH1: V_{OUT}, 200mV/div
CH2: I_{OUT}, 1A/div
TIME: 200μs/div

Short Circuit



CH1: V_{OUT}, 2V/div
CH2: I_{OUT}, 1A/div
TIME: 100μs/div

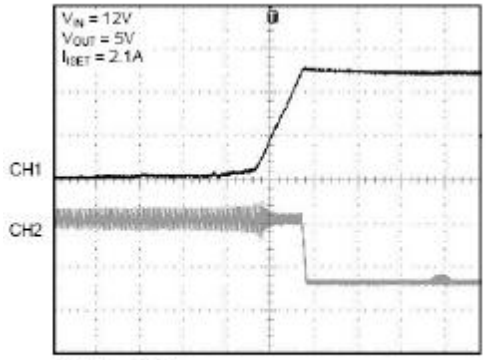
Short Circuit



CH1: V_{OUT}, 2V/div
CH2: I_{OUT}, 1A/div
TIME: 100μs/div

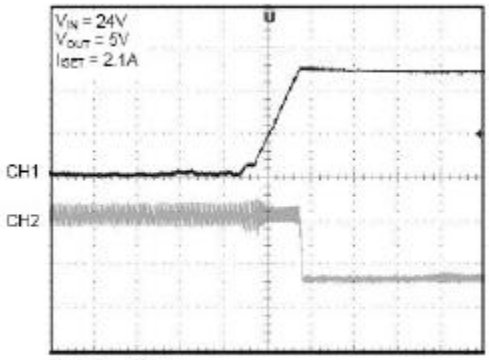
TYPICAL PERFORMANCE CHARACTERISTICS

Short Circuit Recovery



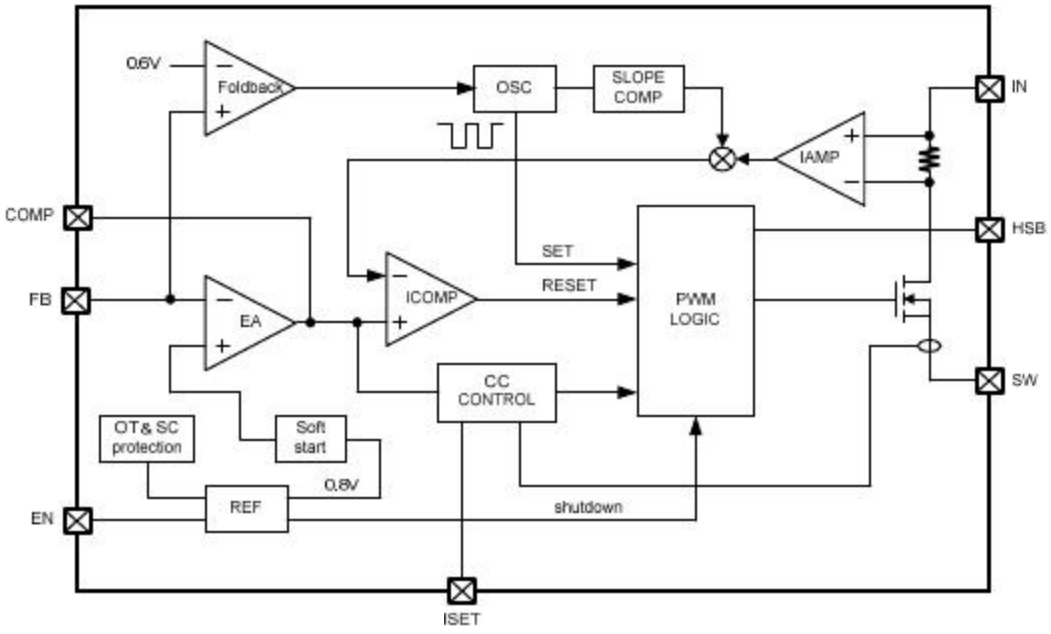
CH1: V_{OUT}, 2V/div
CH2: I_{OUT}, 2A/div
TIME: 1ms/div

Short Circuit Recovery



CH1: V_{OUT}, 2V/div
CH2: I_{OUT}, 2A/div
TIME: 1ms/div

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

CC/CV Loop Regulation

As seen in Functional Block Diagram, the JTM4523 is a peak current mode pulse width modulation (PWM) converter with CC and CV control. The converter operates as follows: A switching cycle starts when the rising edge of the Oscillator clock output causes the High-Side Power Switch to turn on and the Low-Side Power Switch to turn off. With the SW side of the inductor now connected to IN, the inductor current ramps up to store energy in the magnetic field. The inductor current level is measured by the Current Sense Amplifier and added to the Oscillator ramp signal. If the resulting summation is higher than the COMP voltage, the output of the PWM Comparator goes high. When this happens or when Oscillator clock output goes low, the High-Side Power Switch turns off. At this point, the SW side of the inductor swings to a diode voltage below ground, causing the inductor current to decrease and magnetic energy to be transferred to output. This state continues until the cycle starts again. The High-Side Power Switch is driven by logic using HBS as the positive rail. This pin is charged to V_{SW} + 5V when the Low-Side Power Switch turns on. The COMP voltage is the integration of the error between FB input and the internal 0.8V reference voltage. If FB is lower than the reference voltage, COMP tends to go higher to increase current to the output. Output current will increase until it reaches the CC limit set by the ISET resistor. At this point, the device will transition from regulating output voltage to regulating output current, and the output voltage will drop with increasing load. The Oscillator normally switches at 225-KHz. However, if FB voltage is less than 0.6V, then the switching frequency decreases until it reaches a typical value of 30kHz at V_{FB} = 0.15V.

Enable Pin

The JTM4523 has an enable input EN for turning the IC on or off. The EN pin contains a precision 1.6V comparator with 125mV hysteresis and a 10 A pull-up current source. The comparator can be used with a resistor divider from IN to program a startup voltage higher than the normal UVLO value. It can be used with a resistor divider from VOUT to disable charging of a deeply discharged battery, or it can be used with a resistor divider containing a thermistor to provide a temperature-dependent shutoff protection for over temperature battery. The thermistor should be thermally coupled to the battery pack for this usage. If left floating, the EN pin will be pulled up to roughly 5V by the internal

10 A current source. It can be driven from standard logic signals greater than 1.6V, or driven with open-drain logic to provide digital on/off control.

Thermal Shut-Down

The JTM4523 disables switching when its junction temperature exceeds 150°C and resumes when the temperature has dropped by 20°C.

APPLICATION INFORMATION

Setting the output voltage

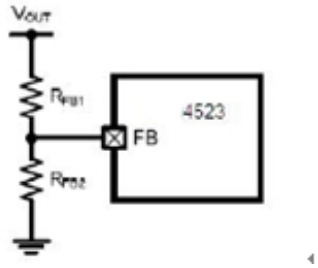


Figure 1, Output Voltage Setting

Figure 1 shows the connections for setting the output voltage. Select the proper ratio of the two feedback resistors RFB1 and RFB2 based on the output voltage. Typically, use RFB2 ≈ 10k and determine RFB1 from the following equation:

$$R_{FB1} = R_{FB2}\left(\frac{V_{OUT}}{0.8V} - 1\right) \quad .. \quad (1)$$

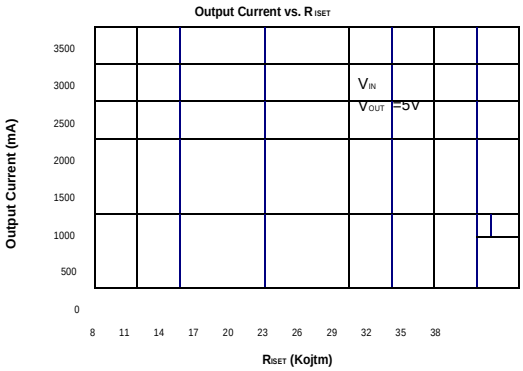


Figure 2, Curve for programmable Output CC Current

CC Current Setting

JTM4523 constant current value is set by a resistor connected between the ISET pin and GND. The CC output current is linearly proportional to the current flowing out of the ISET pin. The voltage at ISET is roughly 1V and the current gain from ISET to output is roughly 25000 (25mA/1 A). To determine the proper resistor for a desired current, please refer to Figure 2 above.

CC Current Line Compensation

When operating at constant current mode, the current limit increase slightly with input voltage. For wide input voltage applications, a resistor RC is added to compensate line change and keep output high CC accuracy, as shown in Figure 3.

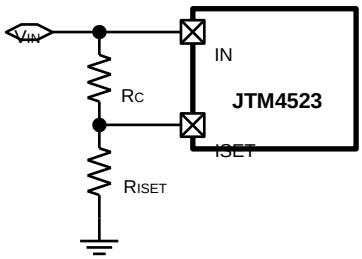


Figure 3, Input Line Compensation

Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value.

Higher inductance reduces the peak-to-peak ripple current. The trade off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value L based on ripple current requirement.

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} f_{sw} I_{LOADMAX} K_{RIPPLE}} \quad \text{... (2)}$$

Where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency, $I_{LOADMAX}$ is the maximum load current, and K_{RIPPLE} is the ripple factor. Typically, choose K_{RIPPLE} = 30% to correspond to the peak-to-peak ripple current being 30% of the maximum load current. With a selected inductor value the peak-to-peak inductor current is estimated as:

$$I_{LPK-PK} = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{L \cdot V_{IN} \cdot f_{sw}} \quad (3)$$

The peak inductor current is estimated as:

$$I_{LPK} = I_{LOADMAX} + \frac{1}{2} I_{LPK-PK} \quad .. \quad (4)$$

The selected inductor should not saturate at I_{LPK}. The maximum output current is calculated as:

$$I_{LPK} = I_{LOADMAX} + \frac{1}{2} I_{LPK-PK} \quad .. \quad (5)$$

L_{LIM} is the internal current limit, which is typically 3.2A, as shown in Electrical Characteristics Table.

External Feed-Through Bias Diode

It is recommended that an external feed-through bias diode be added when the system has a 5V fixed input or the power supply generates a 5V output. This helps improve the efficiency of the regulator. The feed-through bias diode can be a low cost one such as IN4148 or BAT54.

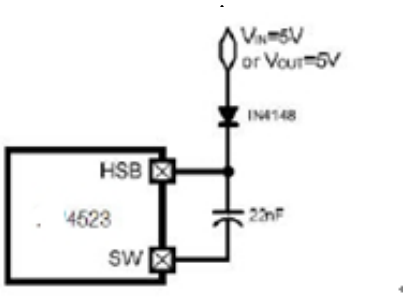


Figure 4, External Feed-Through Bias Diode

Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency. The input capacitance needs to be higher than 10 F. The best choice is the ceramic type, however, low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the IN and GND pins of the IC, with the shortest traces possible. In the case of tantalum or electrolytic types, they can be further away if a small parallel 0.1 F ceramic capacitor is placed right next to the IC.

Output Capacitor

The output capacitor also needs to have low ESR to keep low output voltage ripple. The output ripple voltage is:

$$V_{RIPPLE} = I_{OUTMAX} K_{RIPPLE} R_{ESR} + \frac{1}{28 \cdot f_{SW}^2 L C_{OUT}}$$

Where I_{OUTMAX} is the maximum output current, K_{RIPPLE} is the ripple factor, R_{ESR} is the ESR of the output capacitor, f_{SW} is the switching frequency, L is the inductor value, and C_{OUT} is the output capacitance. In the case of ceramic capacitor, R_{ESR} is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic type. In the case of tantalum or electrolytic capacitors, the ripple is dominated by R_{ESR} multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.

For ceramic output capacitor, typically choose a capacitance of about 22uF. For tantalum or electrolytic capacitors, choose a capacitor with less than 50m ESR.

Rectifier Diode

Use a Schottky diode as the rectifier to conduct current when the High-Side Power Switch is off. The Schottky diode must have current rating higher than the maximum output current and a reverse voltage rating higher than the maximum input voltage.

Stability Compensation

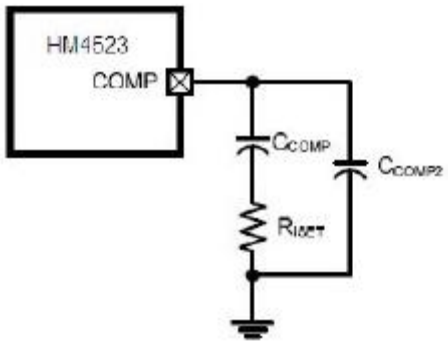


Figure 5, Stability Compensation Network

The feedback loop of the IC is stabilized by the components at the COMP pin, as shown in Figure 5. The DC loop gain of the system is determined by the following equation:

$$A_{VDC} = \frac{V_{FB}\, A_{VEA}}{I_{OUT}\, R_{CS}} \quad .. \quad (7)$$

The dominant pole P1 is due to C_{COMP}:

$$f_{P1} = \frac{G_{EA}}{2\pi\, A_{VEA} C_{COMP}} \quad ... \quad (8)$$

The second pole P2 is the output pole:

$$f_{P2} \quad \frac{1}{2\pi\, R_{OUT} C_{COUT}} \quad .. \quad (9)$$

The first zero Z1 is due to R_{COMP} and C_{COMP}:

$$f_{Z1} = \frac{1}{2\pi\, R_{COMP} C_{COMP}} \quad ... \quad .. \quad (10)$$

And finally, the third pole is due to R_{COMP} and C_{COMP2} (if C_{COMP2} is used):

$$f_{P3} = \frac{1}{2\pi\, R_{COMP} C_{COMP\,2}} \quad ... \quad .. \quad (11)$$

The following steps should be used to compensate the IC:

STEP 1, Set the cross-over frequency at 1/10 of the switching frequency via R_{COMP}:

$$R_{COMP} = \frac{2\pi V_{OUT}\, C_{OUT}\, f_{SW}\, R_{CS}}{10 G_{EA} V_{FB}} \quad .... \quad (12)$$

STEP 2, Set the zero f_{Z1} at 1/4 of the cross-over frequency. If R_{COMP} is less than 15k , the equation for C_{COMP} is:

$$C_{COMP} = \frac{2}{\pi\, R_{COMP}\, f_{SW}} \quad ..... \quad (13)$$

If R_{COMP} is limited to 15k , then the actual cross-over frequency is 6.58 / ($V_{OUT}C_{OUT}$). Therefore:

$$C_{COMP} = \frac{V_{OUT}\, C_{OUT}}{13.16\pi\, R_{COMP} V_{OUT} C_{OUT}} \quad ... \quad (14)$$

STEP 3, If the output capacitor's ESR is high enough to cause a zero at lower than 4 times the cross-over frequency, an additional compensation capacitor C_{COMP2} is required. The condition for using C_{COMP2} is:

$$R_{ESRCOUT} \varepsilon \left(min \frac{1.77 \cdot 10^{6}}{C_{OUT}}, \frac{6 \cdot V_{OUT}}{1000}\right) \quad ... (15)$$

And the proper value for C_{COMP2} is:

$$C_{COMP\,2} = \frac{C_{OUT}\, R_{ESRCOUT}}{R_{COMP}} \quad ..... \quad (16)$$

Though C_{COMP2} is unnecessary when the output capacitor has sufficiently low ESR, a small value C_{COMP2} such as 100pF may improve stability against PCB layout parasitic effects.

Table 1 shows some calculated results based on the compensation method above.

Table 1, Typical Compensation for Different Output Voltages and Output Capacitors

V_{OUT}	C_{OUT}	R_{COMP}	C_{COMP}	C_{COMP2}
2.5V	47uF Ceramic	5.6k	3.3nF	None
3.3V	47uF Ceramic	6.2k	3.3nF	None
5.0V	47uF Ceramic	8.2k	3.3nF	None
2.5V	470uF/6.3V /30m	39k	22nF	47pF
3.3V	470uF/6.3V /30m	45k	22nF	47pF
5.0V	470uF/6.3V /30m	51k	22nF	47pF

Note:
C_{COMP2} is needed for high ESR output capacitor.
C_{COMP2} $\leqslant$ 47pF is recommended.

CC Loop Stability

The constant-current control loop is internally compensated over the 1500mA-3000mA output range, thus no additional external compensation is required to stabilize the CC current.

PCB Layout Guideline

When laying out the printed circuit board (PCB), the following checklist should be used to ensure proper operation of the IC.

1. Arrange the power components to reduce the AC loop size consisting of CIN, IN pin, SW pin and the schottky diode.
2. Place input decoupling ceramic capacitor CIN as close to IN pin as possible. CIN is connected power GND with vias or short and wide path.
3. Return FB, COMP and ISET to signal GND pin, and connect the signal GND to power GND at a single point for best noise immunity. Connect exposed pad to power ground copper area with copper and vias.
4. Use copper plane for power GND for best heat dissipation and noise immunity.
5. Place feedback resistor close to FB pin.
6. Use short trace connecting HSB-CHSB-SW loop.

Figure 6 shows an example of PCB layout.

Figure 7 gives one typical car charger application schematic and associated BOM listed in table 2.

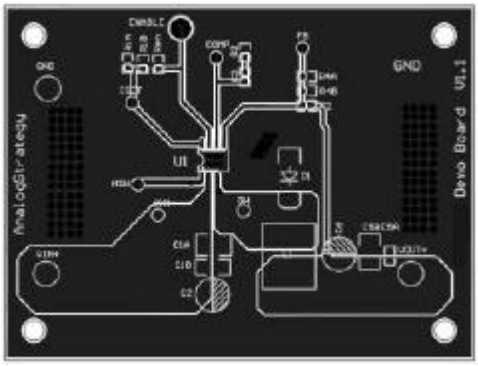


Figure 6(a) Top View of PCB layout

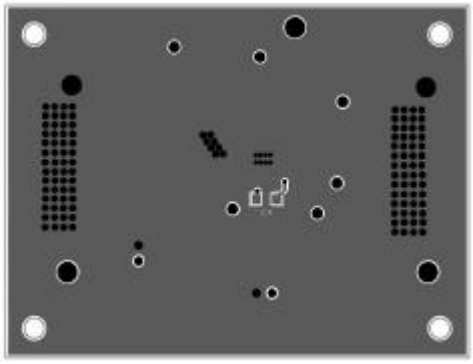


Figure 6(b) Top View of PCB layout

TYPICAL APPLICATION DIAGRAM

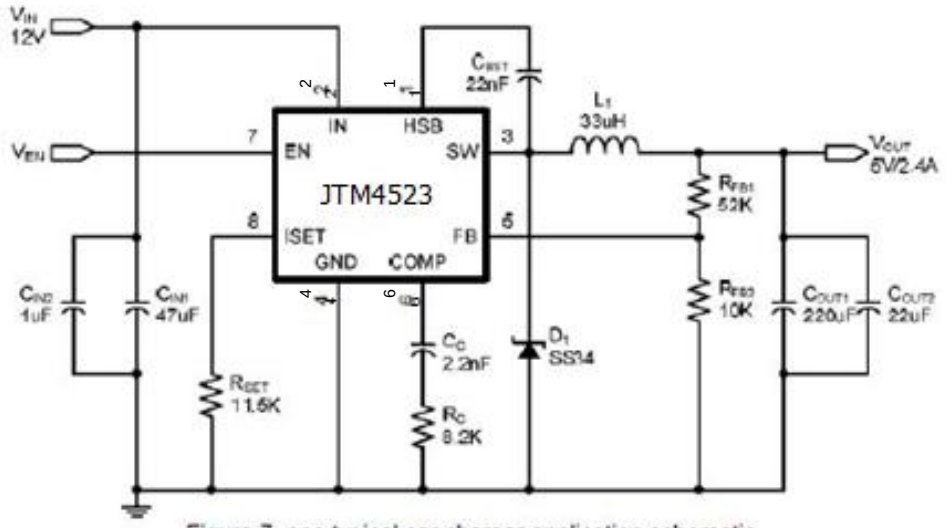


Figure 7, one typical car charger application schematic

Table 2, BOM List for 5V/2.1A Car Charger

ITEM	REFERENCE	DESCRIPTION	MANUFACTURER	QTY
1	U1	IC,HM4523,ESOP8	H&M SEMI	1
2	C_{IN1}	Capacitor,Electrolytic,47uF/50V,6.3x7mm	Murata,TDK	1
3	C_{IN2}	Capacitor,Ceramic,1uF/50V,0805,SMD	Murata,TDK	1
4	C_C	Capacitor,Ceramic,2.2nF/6.3V,0603,SMD	Murata,TDK	1
5	C_{BST}	Capacitor,Ceramic,22nF/50V,0603,SMD	Murata,TDK	1
6	C_{OUT1}	Capacitor, Electrolytic,220uF/10V,6.3x7mm	Murata,TDK	1
7	C_{OUT2}	Capacitor, Ceramic,22uF/10V,1206,SMD	Murata,TDK	1
8	L_1	Inductor,33uH,3A,20%,SMD	Tyco Electronics	1
9	D_1	Diode,Schottky,40V/3A,SS34	MCC	1
10	R_{SET}	Chip Resistor,11.5KΩ,0603,1%	Murata,TDK	1
11	R_{FB1}	Chip Resistor,52KΩ,0603,1%	Murata,TDK	1
12	R_{FB2}	Chip Resistor,10KΩ,0603,1%	Murata,TDK	1
13	R_C	Chip Resistor,8.2KΩ,0603,5%	Murata,TDK	1

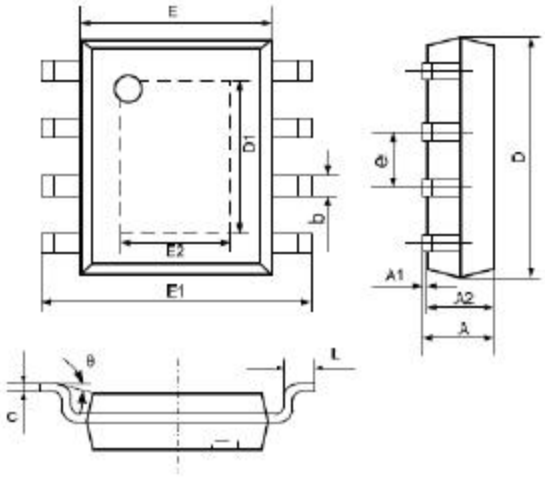
13 Rc Chip Resistor,8.2K,0603,5% Murata,TDK 1

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0.1	Mar-05-2015	Initial Release	--

PACKAGE INFORMATION

SOP-8EP Package Outline Diagram



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.700	0.053	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 TYP		0.050 TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°