

N-Channel Enhancement Mode Power MOSFET

DESCRIPTION

The JTM3307D uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

GENERAL FEATURES

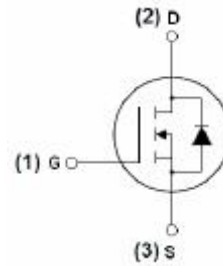
- $V_{DS} = 80V, I_D = 105A$
 $R_{DS(ON)} < 8m\Omega$ @ $V_{GS} = 10V$ (Typ: $6.3m\Omega$)
- High density cell design for ultra low R_{dson}
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

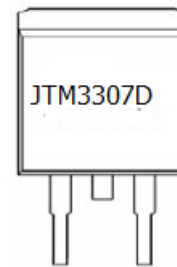
- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

100% UIS TESTED!

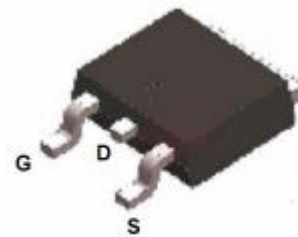
100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin Assignment



TO-263-2L top view

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
JTM3307D	JTM3307D	TO-263-2L	-	-	-

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	105	A
Drain Current-Continuous($T_c = 100^\circ C$)	$I_D (100^\circ C)$	80	A
Pulsed Drain Current	I_{DM}	420	A
Maximum Power Dissipation	P_D	200	W
Derating factor		1.33	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	E_{AS}	800	mJ

Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C
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Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	0.75	°C/W
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Electrical Characteristics (TA=25°C unless otherwise noted)

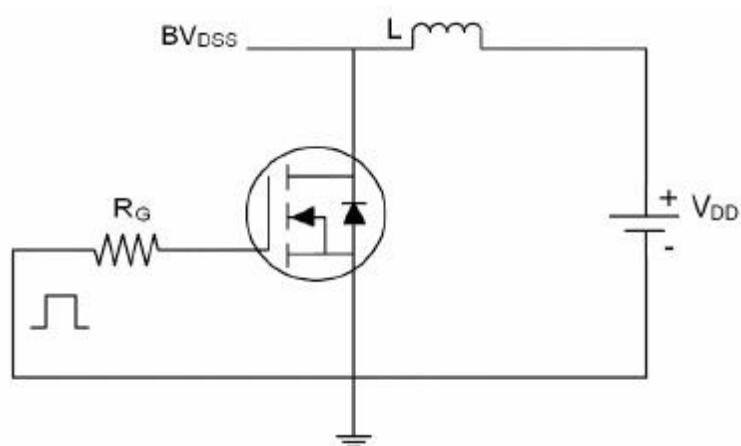
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	80	86	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =80V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	2	3	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =40A	-	6.3	8	mΩ
Forward Transconductance	g _{FS}	V _{DS} =25V,I _D =40A	80	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =25V,V _{GS} =0V, F=1.0MHz	-	4900	-	PF
Output Capacitance	C _{oss}		-	410	-	PF
Reverse Transfer Capacitance	C _{rss}		-	315	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	VDD=30V,ID=2A,RL=15Ω, RG=2.5Ω,VGS=10V	-	20	-	nS
Turn-on Rise Time	t _r		-	19	-	nS
Turn-Off Delay Time	t _{d(off)}		-	70	-	nS
Turn-Off Fall Time	t _f		-	30	-	nS
Total Gate Charge	Q _g	ID=30A,VDD=30V,VGS=10V	-	125	-	nC
Gate-Source Charge	Q _{gs}		-	24	-	nC
Gate-Drain Charge	Q _{gd}		-	49	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =40A	-	-	1.2	V
Diode Forward Current (Note 2)	I _S		-	-	105	A
Reverse Recovery Time	t _{rr}	T _j =25℃,I _F =75A, di/dt=100A/uS (Note3)	-	37		nS
Reverse Recovery Charge	Q _{rr}		-	58		nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

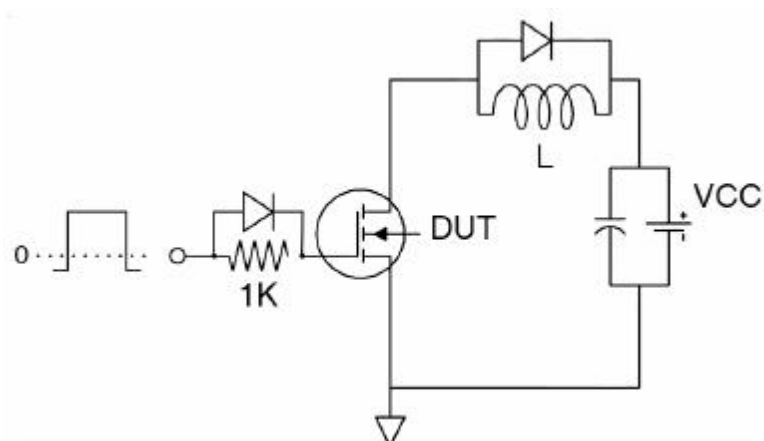
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^\circ C, V_{DD}=40V, V_G=10V, L=0.5mH, R_G=25\Omega$

Test circuit

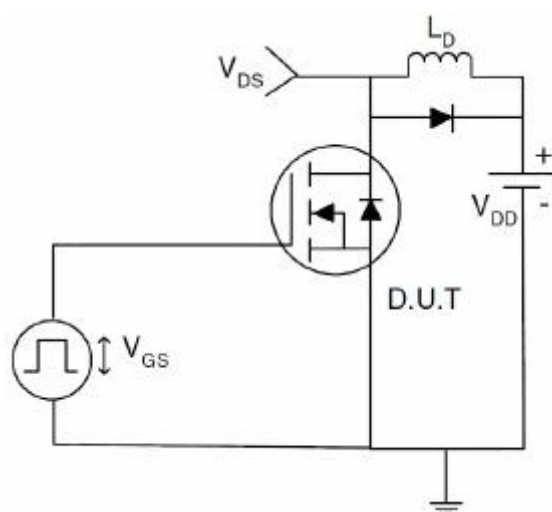
1) EAS test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

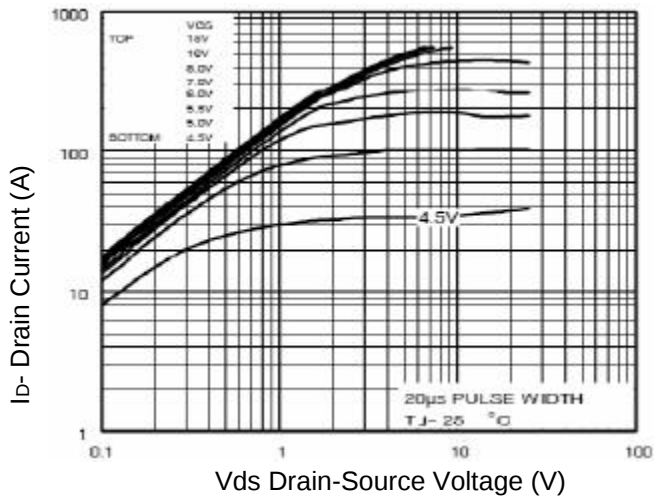


Figure 1 Output Characteristics

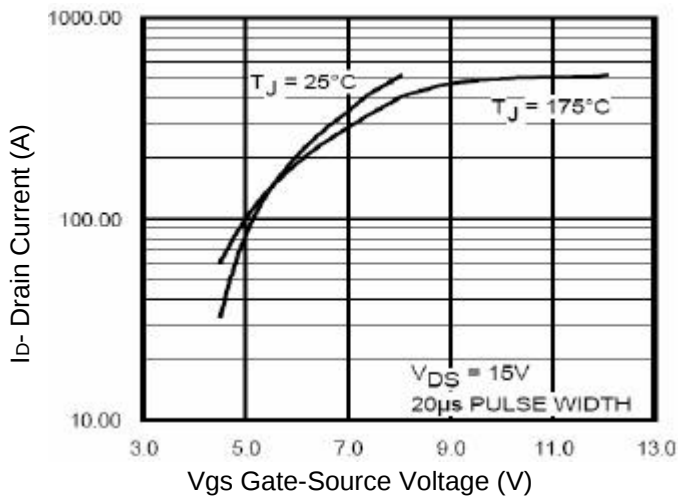


Figure 2 Transfer Characteristics

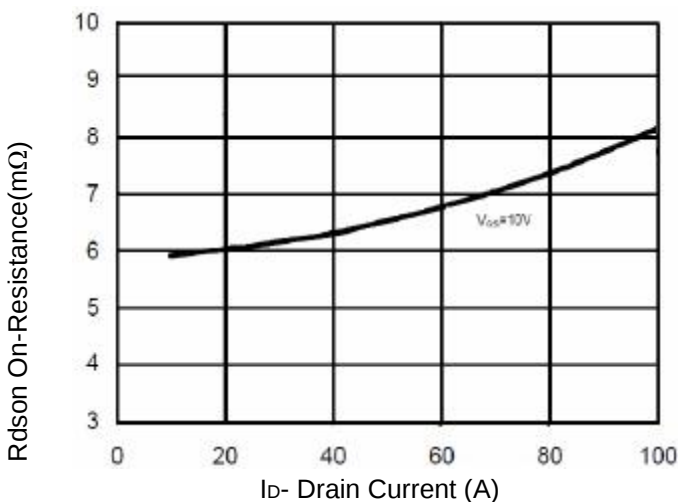
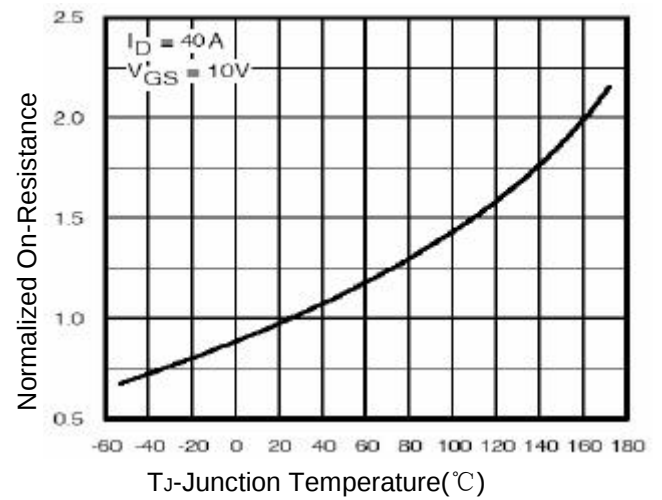
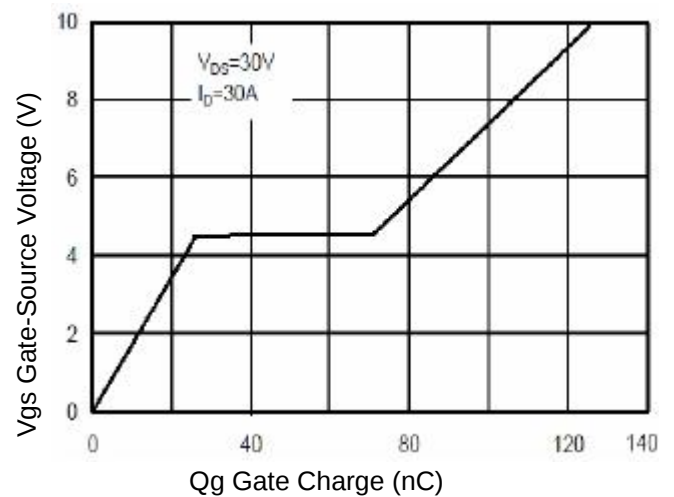
Figure 3 $R_{DS(on)}$ - Drain CurrentFigure 4 $R_{DS(on)}$ -Junction Temperature

Figure 5 Gate Charge

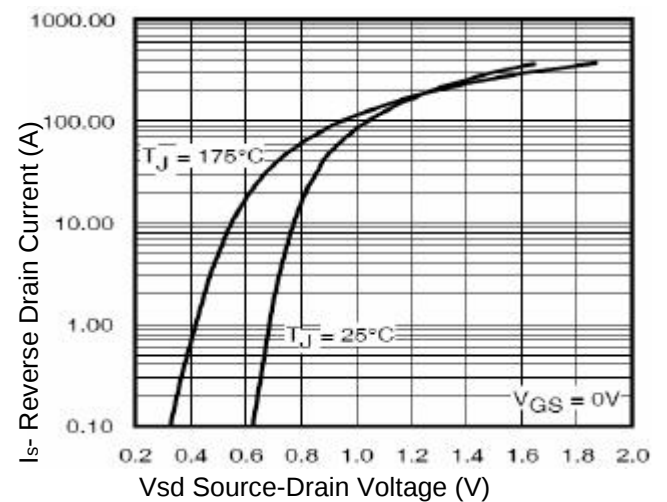


Figure 6 Source- Drain Diode Forward

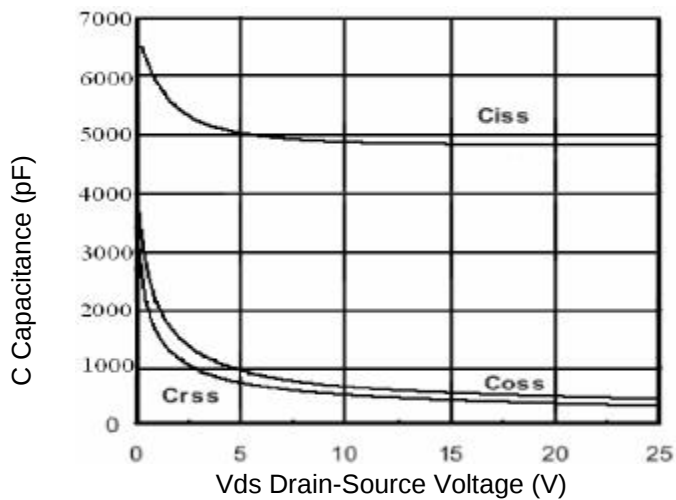


Figure 7 Capacitance vs Vds

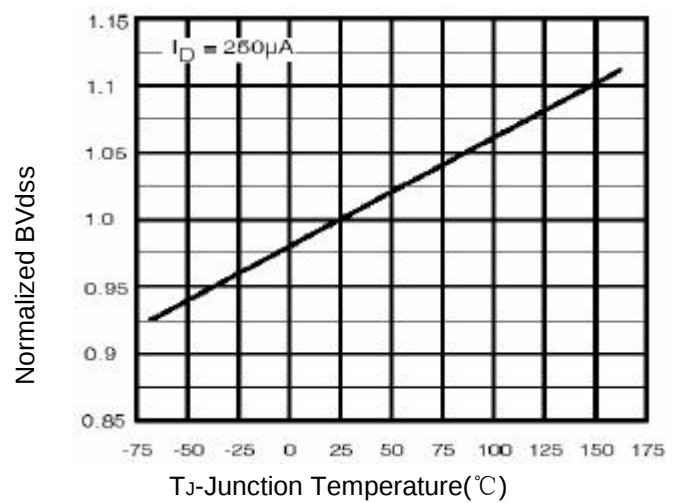
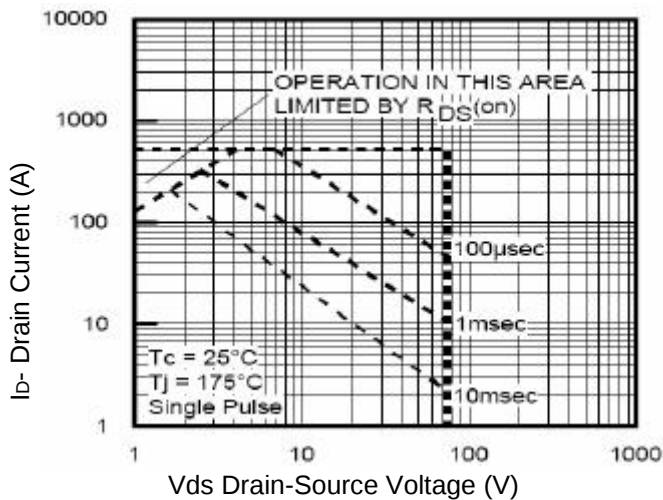
Figure 9 BV_{DSS} vs Junction Temperature

Figure 8 Safe Operation Area

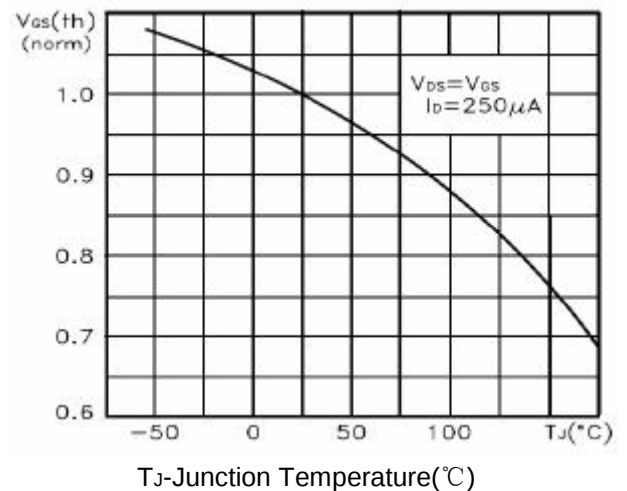
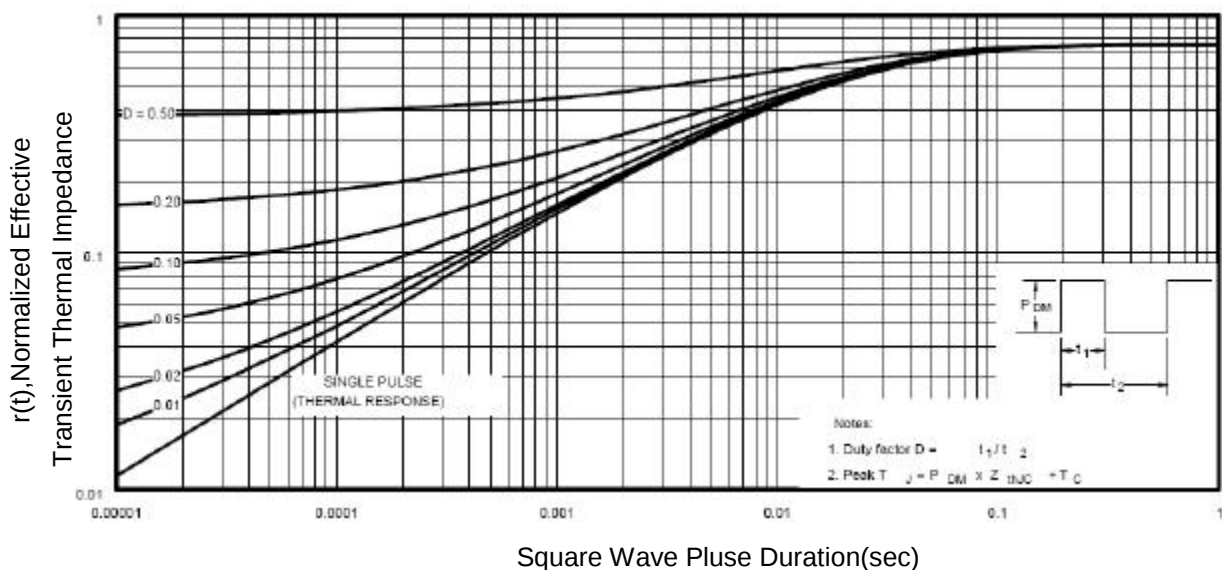
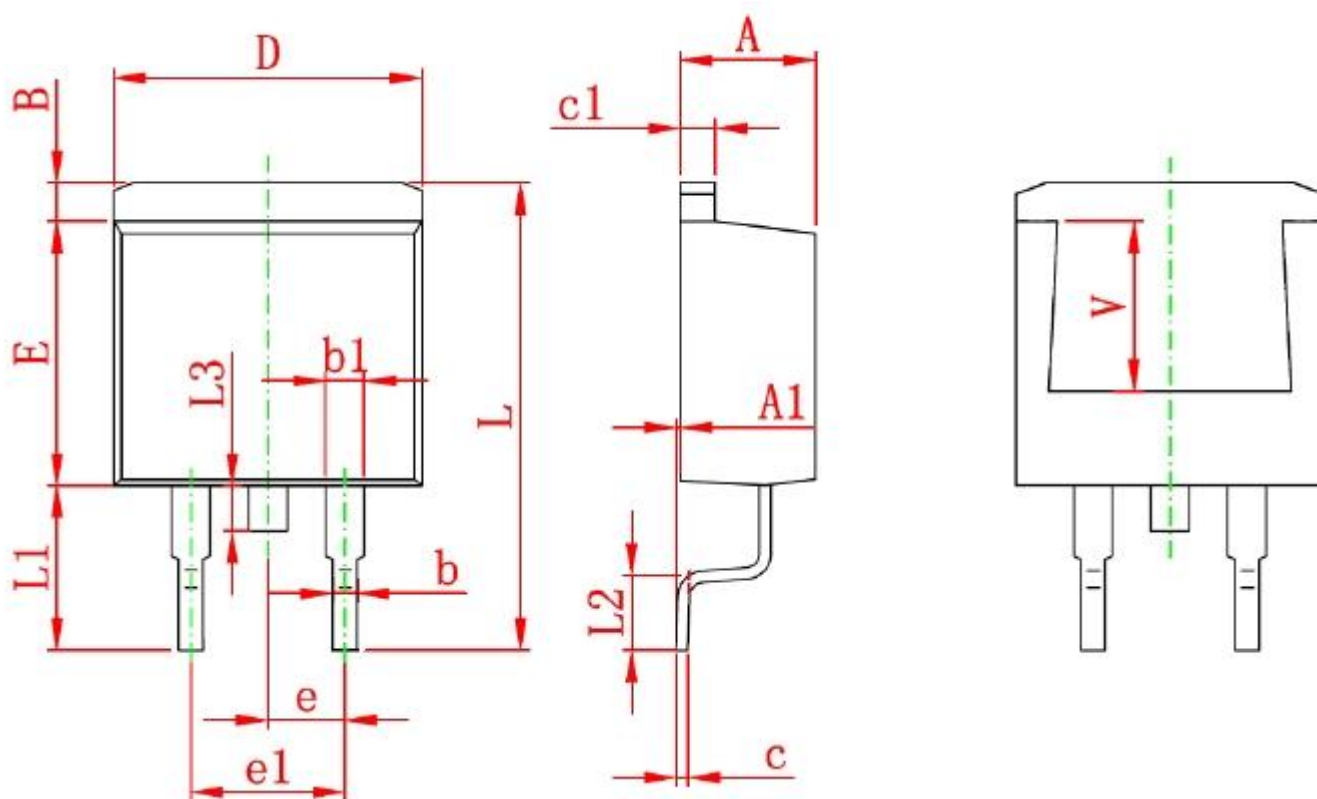
Figure 10 $V_{GS(th)}$ vs Junction Temperature

Figure 11 Normalized Maximum Transient Thermal Impedance

TO-263-2L PACKAGE INFORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.470	4.670	0.176	0.184
A1	0.000	0.150	0.000	0.006
B	1.170	1.370	0.046	0.054
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
E	8.500	8.900	0.335	0.350
e	2.540 (TYP.)		0.100 (TYP.)	
e1	4.980	5.180	0.196	0.204
L	15.050	15.450	0.593	0.608
L1	5.080	5.480	0.200	0.216
L2	2.340	2.740	0.092	0.108
L3	1.300	1.700	0.051	0.067
V	5.600 REF.		0.220 REF.	