1.5MHz, Dual 2A Output Current Synchronous Step-Down Converter

FEATURES

- High Efficiency: Up to 96%
- 1.5MHz Constant Frequency Operation
- Dual 2A Output Current
- No Schottky Diode Required
- 2.3V to 6V Input Voltage Range
- Output Voltage as Low as 0.6V
- 100% Duty Cycle in Dropout
- Low Quiescent Current: 40μA
- Short Circuit Protection
- Thermal Fault Protection
- Inrush Current Limit and Soft Start
- <1μA Shutdown Current
- ESOP8 package

APPLICATIONS

- Set Top Box
- Wireless and DSL Modems
- PDAs
- Computer Peripherals
- Portable Instruments
- Digital Still and Video Cameras

GENERAL DESCRIPTION

The JTM8022 is a 1.5MHz constant frequency current mode, dual high-efficiency PWM step-down converter. It is ideal for portable equipment requiring very high current up t o 2A each channel from single-cell Lithium-ion batteries while still achieving over 90% efficiency during peak load conditions. The JTM8022 also can run at 100% duty cycle for low dropout operation, extending battery life in portable systems while light load operation provides very low output ripple for noise sensitive applications. The JTM8022 can supply up to 2A output load current each channel from a 2.3V to 6V input voltage and the output voltage can be regulated as low as 0.6V. The high switching frequency minimizes the size of external components while keeping switching losses low. The internal slope compensation setting allows the device to operate with smaller inductor values to optimize size and provide efficient operation. The device is available in a Pb-free, 8-Lead ESOP package and is rated over the -40°C to +85°C temperature range.

This device offers two operation modes, PWM control and PFM Mode switching control, which allows a high efficiency over the wider range of the load.

TYPICAL APPLICATION

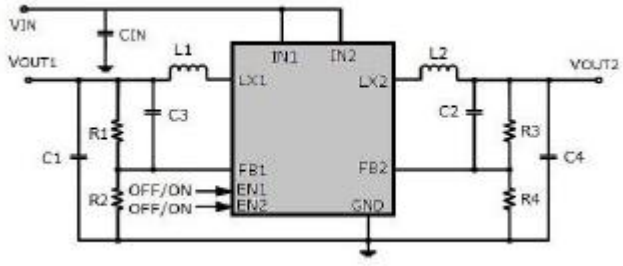
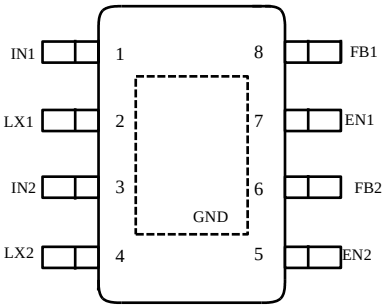


Figure 1. Basic Application Circuit

PIN CONFIGURATION



ESOP8
(JTM8022)

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	VIN1	Power Input of Channel1
2	LX1	Pin for Switching of Channel1
3	VIN2	Power Input of Channel2
4	LX2	Pin for Switching of Channel2
5	EN2	Chip Enable of Channel2
6	FB2	Feedback Input of Channel2
7	EN1	Chip Enable of Channel1
8	FB1	Feedback Input of Channel1
	GND	Ground, The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage VINx -0.3V to 6.5V
ENx,VFBx Voltages.…-0.3 to (Vin+0.3V)
LXx Voltage … ……-0.3V to (Vin+0.3V)
Operating Temperature Range …-40°C to +85°C
Lead Temperature(Soldering,10s) ……..+300°C
Storage Temperature Range ……-65°C to 150°C

THERMAL INFORMATION (Note 2)

Thermal Resistance.....45°C/W M aximum Thermal Dissipation at Ta= 25°C

ELECTRICAL CHARACTERISTICS (Note 3)

(V_{INx}=V_{ENx}=3.6V, V_{OUT}=1.8V, L=2.2uH, Cin=4.7uF, Cout=10uF,T_A = 25°C,unless otherwise noted.)

Parameter	Conditions	MIN	TYP	MAX	unit
Channel1 and Channel2					
Input Voltage Range		2.3		6	V
UVLO Threshold		1.7	1.9	2.1	V
Input DC Supply Current	(Note 4)				μA
PWM Mode	Vout = 90%, ILoad=0mA		150	300	μA
PFM Mode	Vout = 105%, ILoad=0mA		40	75	μA
Shutdown Mode	V_{EN} = 0V, V_{IN}=4.2V		0.1	1.0	μA
Regulated Feedback Voltage V_{FBx}	T_A = 25°C	0.588	0.600	0.612	V
	T_A = 0°C ≤ T_A ≤ 85°C	0.586	0.600	0.613	V
	T_A = -40°C ≤ T_A ≤ 85°C	0.585	0.600	0.615	V
Reference Voltage Line Regulation	Vin=2.5V to 5.5V		0.1		%/V
Output Voltage	V_{IN} = 2.5V to 5.5V, Iout=10mA to 2000mA	-3		+3	%Vout
Output Voltage Load Regulation	Iout=10mA to 2000mA		0.2		%/A
Oscillation Frequency	Vout=100%		1.5		MHz
	Vout=0V		300		KHz
On Resistance of PMOS	I_{LX}=100mA		100	150	mΩ
On Resistance of NMOS	I_{LX}=-100mA		90	150	mΩ
Peak Current Limit	V_{INx}= 3V, Vout=90%		4		A
EN Threshold		0.30	1.0	1.50	V
EN Leakage Current			±0.01	±1.0	μA
SW Leakage Current	V_{ENx}=0V,V_{INx}=Vsw=5V		±0.01	±1.0	μA

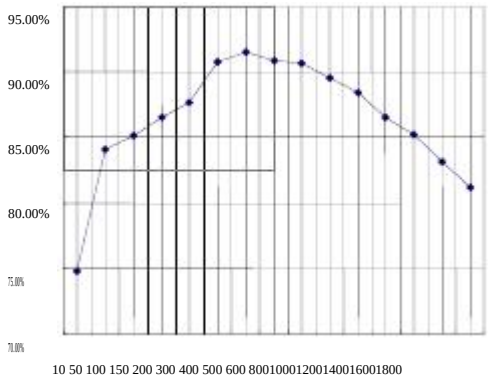
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = TA + (PD) \times (250°C/W)$.

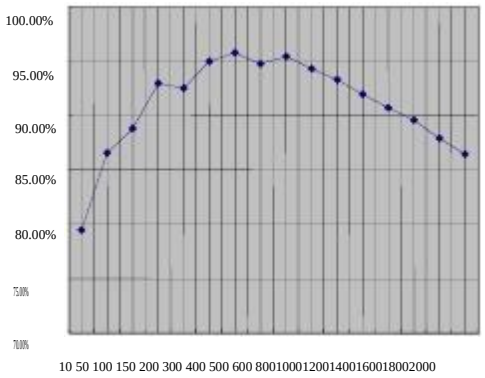
Note3: 100% production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

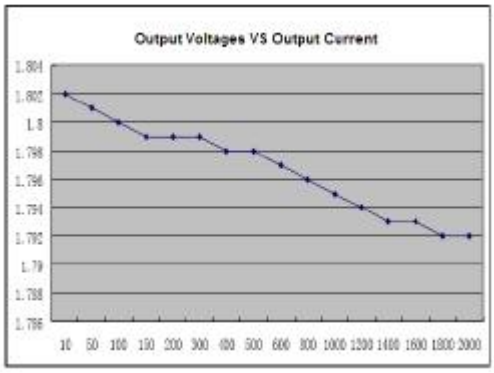
TYPICAL PERFORMANCE CHARACTERISTICS



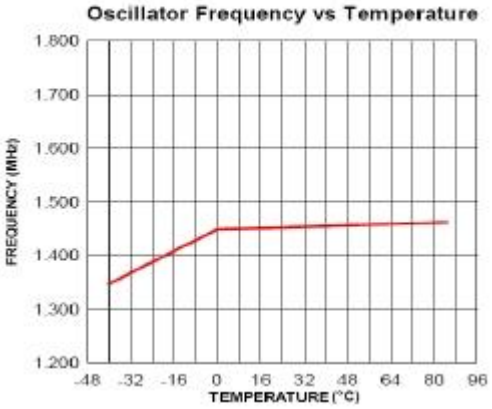
Vin=5V, Vout=1.8V

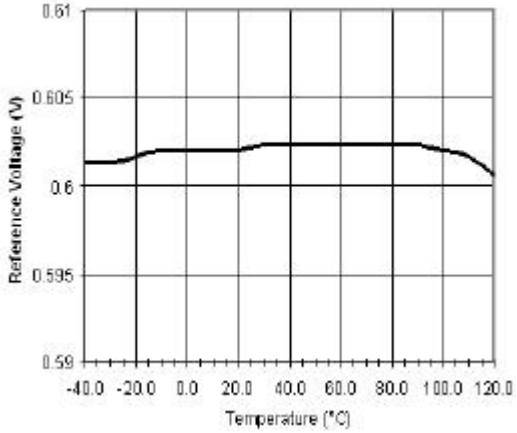


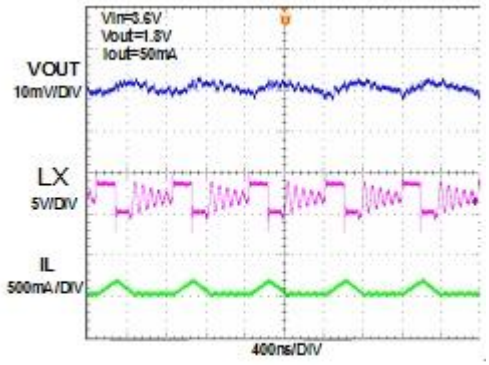
Vin=5V, Vout=3.3V



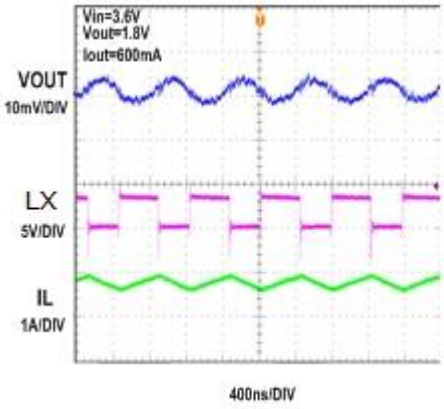
Vin=3.6V Vout=1.8V



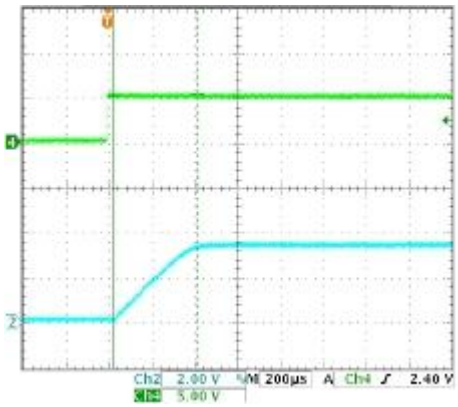




PFM MODE



PWM MODE



Start Up

FUNCTIONAL BLOCK DIAGRAM

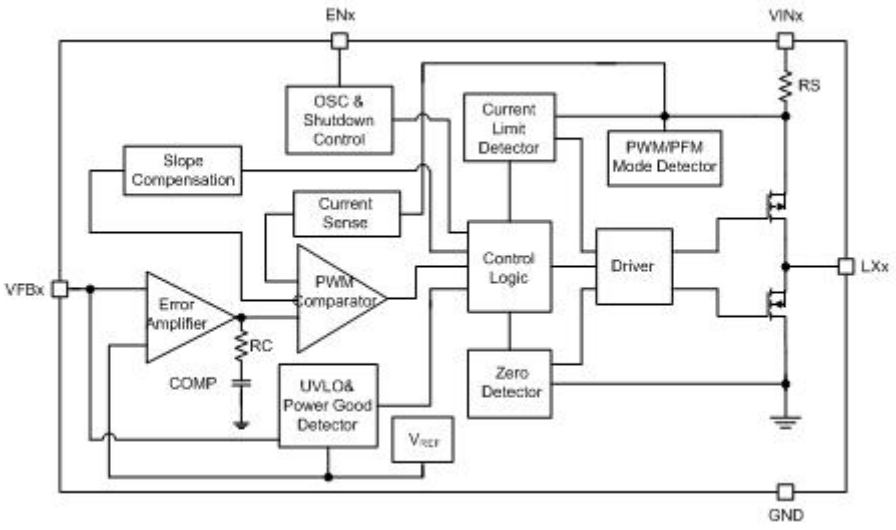


Figure 2. JTM8022 Block Diagram

FUNCTIONAL DESCRIPTION

The JTM8022 is a dual high output current monolithic switch mode step-down DC-DC converter. The device operates at a fixed 1.5MHz switching frequency, and uses a slope compensated current mode architecture. This step-down DC-DC converter can supply up to dual respective 2000mA output current at VIN = 3.6V and has an input voltage range from 2.3V to 6V. It minimizes external component size and optimizes efficiency at the heavy load range. The slope compensation allows the device to remain stable over a wider range of inductor values so that smaller values (1μH to 4.7μH) with lower DCR can be used to achieve higher efficiency. Only a small bypass input capacitor is required at the output. The adjustable version can be programmed with external feedback to any voltage, ranging from 0.6V to nearly the input voltage. It uses internal MOSFETs to achieve high efficiency and can generate very low output voltages by using an internal reference of 0.6V. At dropout, the converter duty cycle increases to100% and the output voltage tracks the input voltage minus the low RDS(ON) drop of the P-channel high-side MOSFET and the inductor DCR. The internal error amplifier and compensation provides excellent transient response, load and line regulation. Internal soft start eliminates any output voltage overshoot when the enable or the input voltage is applied.

Setting the Output Voltage

Figure 1 s hows the basic application circuit for the JTM8022. The JTM8022 can be externally programmed. Resistors R1(Or R3) and R2(Or R4) in Figure 1 program the output to regulate at a voltage higher than 0.6V. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R2(Or R4) is 59kΩ. Although a larger value will further reduce quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Table 1 summarizes the resistor values for various output voltages with R2 set to either 59kΩ for good noise immunity or 316kΩ for reduced no load input current.
The JTM8022, combined with an external feed forward capacitor (Cin in Figure 1), delivers enhanced transient response for extreme pulsed load applications. The addition of the feed forward capacitor typically requires a larger output capacitor Cout for stability. The external resistor sets the output voltage according to the following equation:

$$V_{OUT} = 0.6 \cdot (1 + \frac{R_1}{R_2})$$

$$R_1 = (V_{OUT} / 0.6 \square 1) \cdot R_2$$

Table 1 shows the resistor selection for different output voltage settings.

V_{OUT} (V)	R2 = 59kΩ R1 (kΩ)	R2 = 316kΩ R1 (kΩ)
0.8	19.6	105
0.9	29.4	158
1.0	39.2	210
1.1	49.9	261
1.2	59.0	316
1.3	68.1	365
1.4	78.7	422
1.5	88.7	475
1.8	118	634
1.85	124	655
2.0	137	732
2.5	187	1000
3.3	267	1430

Table 1: Resistor selections for different output voltage settings (standard 1% resistors substituted for calculated values).

APPLICATIONS INFORMATION

Inductor Selection

For most designs, the JTM8022 operates with inductors of 1μH to 4.7μH. Low inductance values are physically smaller but require faster switching, which results in some efficiency loss. The inductor value can be derived from the following equation:

$$L = \frac{V_{OUT} \cdot (V_{IN} \square V_{OUT})}{V_{IN} \cdot \square I_L \cdot f_{OSC}}$$

Where $\square I_L$ is inductor Ripple Current. Large value inductors result in lower ripple current and small value inductors result in high ripple current. For optimum voltage-positioning load transients, choose an inductor with DC series resistance in the 50mΩ to 150mΩ range.

Manufactu	Part Number	Ind (uH)	DCR (Ojtm)	Max DC Curre	Size L*W*H(mm3)
Sumida	CDRH5D16	2.2	28.7	3	5.8x5.8x1.8
		3.3	35.6	2.6	
		4.7	19	3.4	8.3x8.3x3.0
Sumida	CDRH5D16	2.2	23	3.3	5.2x5.2x3.
		3.3	29	2.6	
		4.7	39	2.1	

Table2.Recommend Surface Mount Inductors

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. T he input capacitor impedance at the switching frequency should be less than input source impedance to prevent high frequency switching current passing to the input. A low ESR input capacitor sized for maximum RMS current must be used. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and s mall temperature coefficients. A 22μF ceramic capacitor for most applications is sufficient. A large value may be used for improved input voltage filtering.

Output Capacitor Selection

The output capacitor is required to keep the output voltage ripple small and to ensure regulation loop stability. The output capacitor must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and high ripple current ratings. The output ripple V_{OUT} is determined by:

$$\square V_{OUT} \delta \quad \frac{V_{OUT} \cdot (V_{IN} \square V_{OUT})}{V_{IN} \cdot f_{OSC} \cdot L} \cdot \left(ESR + \frac{1}{8 \cdot f_{osc} \cdot C3} \right)$$

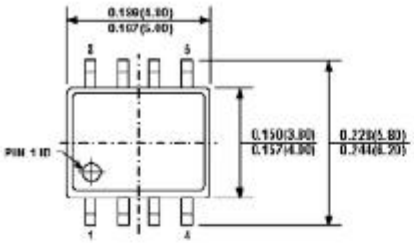
A 22μF ceramic can satisfy most applications.

PC Board Layout Checklist

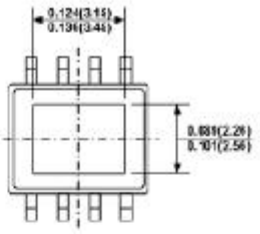
When laying out the Printed Circuit board, the following layout guideline should be followed to ensure proper operation of the JTM8022:

1. The exposed pad (EP) must be reliably soldered to the GND plane.
2. The power traces, including the GND trace, the LX trace and the VIN trace should be kept short, direct and wide to allow large current flow. The L connection to the LX pins should be as short as possible. Use several VIA pads when routing between layers.
3. The input capacitor (Cin) should connect as closely as possible to VIN an d GND to get good power filtering.
4. Keep the switching node, LX away from the sensitive FB/VOUT node.
5. The feedback trace or VOUT pin should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation. If external feedback resistors are used, they should be placed as closely as possible to the FB pin to minimize the length of the high impedance feedback trace.
6. The output capacitor Cout and L s hould be connected as closely as possible. The connection of L to the LX pin should be as short as possible and there should not be any signal lines under the inductor.
7. The resistance of the trace from the load return to GND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.

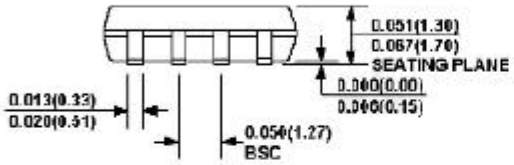
PACKAGE DESCRIPTION



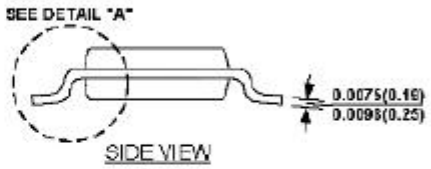
TOP VIEW



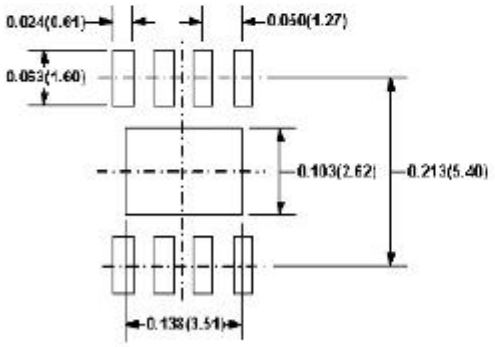
BOTTOM VIEW

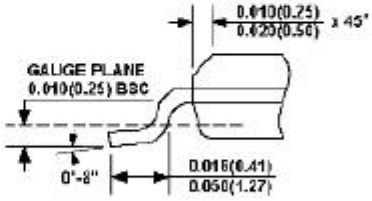


FRONT VIEW



SIDE VIEW





DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.