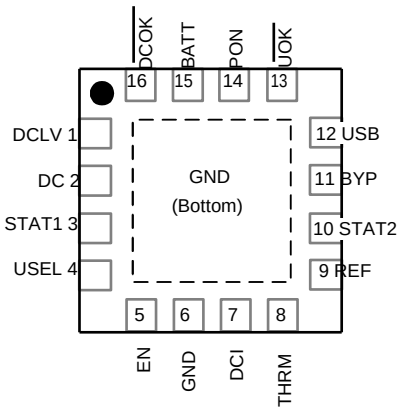
JTMA3200

Dual-Input, USB/AC Adapter, 1-Cell
Li+ Charger with OVP and Thermal Regulation

Features

- **Charge from USB or AC Adapter**
- **Accurate BATT Regulation Voltage**
- **Programmable DC Charging Current**
- **Selectable USB Charging Current (Either 100mA or 500mA)**
- **Thermal Regulation for Simplified Board Design**
- **Input Protection Up to 18V**
- **Soft-Start**
- **External Thermistor Monitoring**
- **Charge Shutdown Control**
- **Charge Status Outputs**
- **DC and USB Power-OK Indicators**
- **Small, High Power QFN5x5-16 and TQFN4x4-16 Packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Pin Configuration



JTMA3200
(Top View)

General Description

The JTMA3200 charges a single-cell Li+ battery from both USB and AC adapter sources. It also includes battery-to-input power switchover, therefore, the system can be powered directly from the power source rather than from the battery.

In its simplest application, the JTMA3200 doesn't need external MOSFET or diodes and accepts input voltages up to 6.5V; however, DC input over-voltage protection up to 18V can be added with a single SOT PFET.

On-chip thermal limiting simplifies PC board layout and allows optimum charging rate without the thermal limits imposed by worst-case battery and input voltage. When the JTMA3200 thermal limit is reached, the charger does not shut down but simply reduces charging current. Ambient or battery temperature can be monitored with an external thermistor. When the temperature is out of range, charging pauses.

Other features include STAT 1 and STAT 2 outputs indicating various charge status. DC power-OK ($\overline{\text{DCOK}}$), USB power-OK ($\overline{\text{UOK}}$), and poweron (PON) outputs indicate when valid power is present. These outputs drive logic or power-selection MOSFETs to disconnect the charging sources from the load and to protect the JTMA3200 from overvoltage. The JTMA3200 doesn't contain logic for communication with the USB host. It must receive instructions from a local microcontroller. The JTMA3200 is available in 16-pin 5mmx5mm QFN and 4mmx4mm TQFN packages and operates over the -40°C to +85°C temperature range.

Applications

- **Smart Phones and PDAs**
- **Wireless Appliances**
- **Digital Still Camera**
- **Internet Appliances**

Ordering and Marking Information

JTMA3200 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QA : QFN5x5-16 QB : TQFN4x4-16 Operating Ambient Temperature Range I : -40 to 85 C° Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device

JTMA3200 QA/QB:	JTMA320 0	XXXXX - Date Code

Note: JIATAIMU lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. JIATAIMU lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. JIATAIMU defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
	DC, DCOK to GND	-0.3 ~ 20	V
	DCLV, USB, BATT, UOK, PON, STAT1, STAT2, EN, USEL to GND	-0.3 ~ 7	V
V_{BYP}	BYP to GND	-0.3 ~ 7	V
	DCI, THRM, REF to GND	-0.3 ~ V_{BYP}+0.3V	V
	Continuous DCLV Input Current	1.6	A
	Continuous USB Input Current	0.6	A
	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance (Note 2) QFN5x5-16 TQFN4x4-16	40	°C/W

Note 2 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of QFN-16 is soldered directly on the PCB.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{DC}	DC Input Voltage (with OVP Protection)	4.35 ~ 18	V
V_{DC}, V_{DCLV}	DCLV Input Voltage (without OVP Protection)	4.35 ~ 6.0	V
V_{USB}	USB Input Voltage	4.35 ~ 6.5	V

Recommended Operating Conditions (Cont.)

Symbol	Parameter	Range	Unit
	DCLV Input Current	~1	A
	USB Input Current	~ 0.5	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Electrical Characteristics

Refer to the typical application circuit. These specifications apply over $V_{USB}=V_{DC}=V_{DCLV}=V_{EN}=V_{USEL}=5V$, $V_{BATT}=4.2V$ and T_A= -40~85°C (T_J= -40~125°C), unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	JTMA3200			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{DC}	DC Supply Current	V_{EN} = 0V	-	1	2	mA
		V_{EN} = 5V, I_{CHG_DC}=0A		1	2	mA
I_{DCLV}	DCLV Supply Current	V_{EN} = 0V, V_{DCLV} = 5V, V_{USB} = 0V	-	300	500	∝A
		V_{EN} = 5V, V_{DCLV} = 5V, V_{USB} = 0V	-	2	3	mA
I_{USB}	USB Supply Current	V_{EN} = 0V, V_{USB} = 5V, V_{DCLV} = 0V	-	300	500	∝A
		V_{EN} = 5V, V_{USB} = 5V, V_{DCLV} = 0V I_{CHG_USB}=0A	-	2	3	mA
		V_{USB}<V_{DCLV}	-	80	160	∝A
DC POWER-OK VOLTAGE THRESHOLD AND TIMING						
	Rising DC Power-OK Threshold		3.45	3.65	3.85	V
	DC Power-OK Hysteresis		0.1	0.15	0.2	V
	DC Rising to DCOK Falling and PON Rising (90%)	V_{DC} rising to 5V, V_{USB}=open	-	20	-	ms
	DC Rising to UOK and PON Going to Open-Drain	V_{DC} step to 5V, V_{USB}= 5V	-	10	-	ms
	DC Falling to DCOK and PON Going to Open-Drain Propagation Delay	V_{USB}=0V or 5V	-	1	-	∝s
USB POWER-OK VOLTAGE THRESHOLD AND TIMING						
	Rising USB Power-OK Threshold		3.45	3.65	3.85	V
	USB Power-OK Hysteresis		0.1	0.15	0.2	V
	USB Rising to UOK Falling and PON Rising	V_{DC}=0V, V_{USB} step to 5V	-	20	-	ms
	USB Falling to UOK and PON Going to Floating Propagation Delay	V_{DC}=0V	-	1	-	∝s
CHARGING POWER-OK VOLTAGE THRESHOLDS						
	Rising DCLV Charging Power-OK Threshold		3.90	4.05	4.2	V
	DCLV Charging Power-OK Hysteresis		0.15	0.25	0.35	V
	Rising USB Charging Power-OK Threshold		3.90	4.05	4.2	V
	USB Charging Power-OK Hysteretic		0.15	0.25	0.35	V

Electrical Characteristics (Cont.)

Refer to the typical application circuit. These specifications apply over V_{USB}=V_{DC}=V_{DCLV}=V_{EN}=V_{USEL}=5V, V_{BATT}=4.2V and T_A= -40~85°C (T_J= -40~125°C), unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	JTMA3200			Unit
			Min.	Typ.	Max.	
BATTERY VOLTAGE AND REFERENCE VOLTAGE						
	BATT Regulation Voltage		-	4.20	-	V
	BATT Regulation Voltage Accuracy	T_A=25°C, V_{BYP}=4.0~6.5V	-0.5	-	0.5	%
		T_A=-40~85°C (T_J=-40°~125 C)	-1	-	1	%
	BATT Pre-qual Voltage Threshold		2.8	3	3.2	V
	Pre-qual Threshold Hysteresis		-	70	-	mV
	REF Regulation Voltage		-	3	-	V
	REF Voltage Accuracy	I_{REF}=0~500∝A,T_J=-40~125°C, V_{BYP}=4.0V~6.5V	-2	-	2	%
	REF Maximum Output	REF=GND	-	1.5	-	mA
BATTERY CHARGING AND PRECHARGING CURRENT						
I_{CHG_DC}	DC Charging Current Range	I_{CHG_DC}=K_{SET} x V_{SET} / R_{SET}, Without thermal regulation	100	-	1500	mA
V_{SET}	DCI Regulation Voltage	Without thermal regulation	-	1	-	V
	DCI Regulation Voltage Accuracy	T_J=-40~125°C, V_{BYP}=4.0~6.5V	-1	-	1	%
	Maximum DCI Output Current	DCI=GND	-	1.8	-	mA
K_{SET}	Charging Current Set Factor	100mAδI_{CHG_DC}δ1A	940	1000	1060	-
I_{CHG_USB}	USB Charging Current	V_{USEL}=0V	70	82	95	mA
		V_{USEL}=5V	400	450	495	mA
	Pre-qual charging Current	V_{BATT}= 0 ~ 3V	35	55	70	mA
	Charge-Done Current Threshold	DC Input, falling charging current (% of charger current set at DCI)	8	12.5	19	%
		Hysteresis	-	12.5	-	%
		USB Input, V_{USEL}=5V, Falling charging current (% of USB charger current)	20	25	30	%
		Hysteresis	-	25	-	%
		USB Input, V_{USEL}=0V	In Voltage Mode			-
DROPOUT VOLTAGES						
	DCLV to BATT Dropout Voltage	I_{CHG_DC}=1A, V_{DCLV}=5V	-	250	450	mV
	USB to BATT Dropout Voltage	I_{CHG_USB}=450mA, V_{USB}=5V	-	140	250	mV
	DCLV to BYP Dropout Voltage	$I_{DCLV\text{-}to\text{-}BYP}$=5mA, V_{DCLV}=5V	-	300	-	mV
	USB to BYP Dropout Voltage	$I_{USB\text{-}to\text{-}BYP}$=5mA, V_{USB}=5V,V_{DCLV}=0V	-	300	-	mV
THERMISTOR MONITOR AND DIE TEMPERATURE REGULATION						
	THRM Cold Trip Level	V_{THRM} rising	0.79	0.81	0.82	V_{REF}
	THRM Cold Trip Level Hysteresis		-	0.03	-	V_{REF}
	THRM Hot Trip Level	V_{THRM} falling	0.28	0.29	0.30	V_{REF}
	THRM Hot Trip Level Hysteresis		-	0.03	-	V_{REF}
	Die Thermal Regulation Limit		-	120	-	°C
	THRM Disable Voltage Threshold		50	100	150	mV

Electrical Characteristics (Cont.)

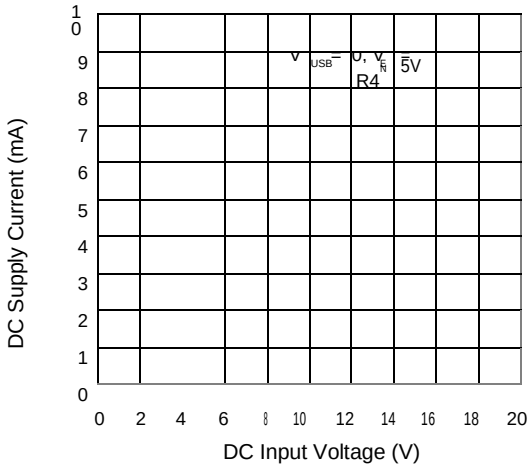
Refer to the typical application circuit. These specifications apply over $V_{USB}=V_{DC}=V_{DCLV}=V_{EN}=V_{USEL}=5V$, $V_{BATT}=4.2V$ and T_A= -40~85°C (T_J= -40~125°C), unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	JTMA3200			Unit
			Min.	Typ.	Max.	
SOFT-START, DC OVER-VOLTAGE VOLTAGE THRESHOLD, AND REVERSE CURRENT						
T_{SS}	Soft-Start Interval	I_{CHG}=0A to fast-charging current	4	7	12	ms
	Rising DC Over-Voltage Threshold		6.2	6.4	6.6	V
	BATT Input Current	$V_{DCLV}=V_{USB}$=0V, V_{BATT}=4.2V	-	-	8	∝A
	BATT Shutdown Input Current	V_{EN}=0V, V_{DCLV} and/or V_{USB}=5V, V_{BATT}=4.2V	-	-	4	∝A
LOGIC INPUT/OUTPUTS AND GATE DRIVERS						
	PON Pull-High Resistance	PON pulled up to BYP	-	10	-	&
	PON Pull-low Resistance	PON pulled to GND, $V_{DCLV}=V_{USB}$=0V	-	140	-	k&
	DCOK, UOK, STAT1, STAT2 Pull-low Resistance	All pins pulled to GND	-	10	-	&
	DCOK Off-Leakage Current	V_{DCOK}=12V, VDC=0V	-	-	1	∝A
	UOK Off-Leakage Current	V_{UOK}=5V, VDC=5V	-	-	1	∝A
	STAT1, STAT2 Off-Leakage Current	$V_{STAT1,2}$=5V, $V_{DC}=V_{USB}$=0V	-	-	1	∝A
	EN, USEL Logic-Input High Level	T_J=-40~125°C, rising	1.6	-	-	V
	EN, USEL Logic-Input Low Level		-	-	0.4	V
	EN, USEL Input Bias Current		-	-	1	∝A

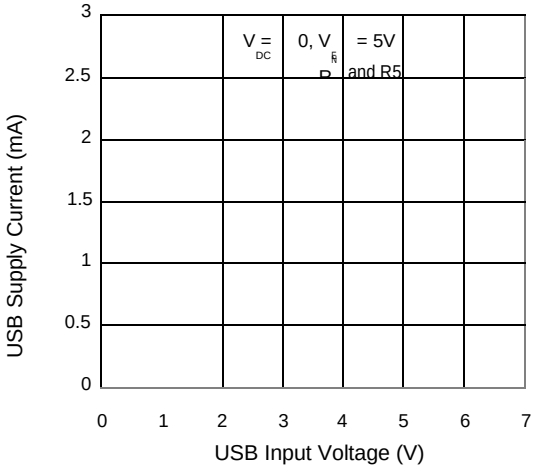
Typical Operating Characteristics

(V_{USB}=V_{DC}=V_{DCLV}=V_{EN}=5V, V_{BATT}=4.2V, V_{THRM}=$V_{REF/2}$, V_{USEL}=5V, Typical Application Circuit 3, T_A=25°C, unless otherwise noted)

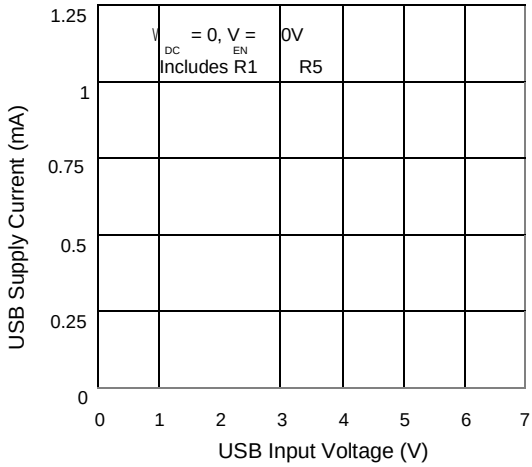
DC Supply Current vs. DC Input Voltage



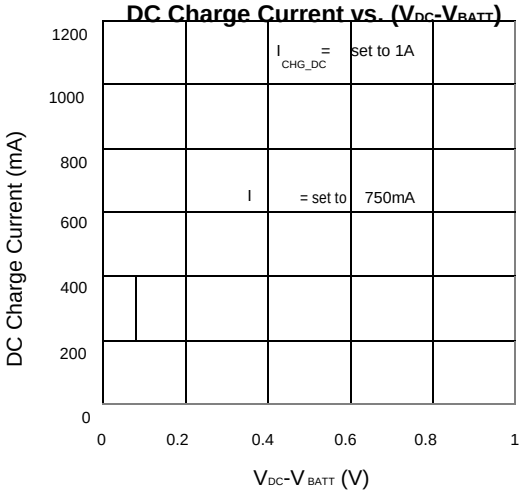
USB Supply Current vs. USB Input Voltage



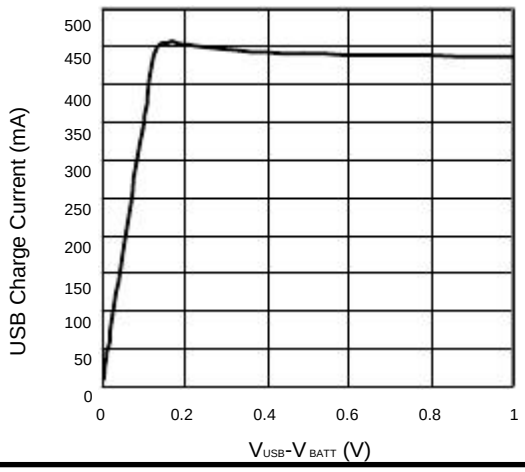
USB Supply Current vs. USB Input Voltage



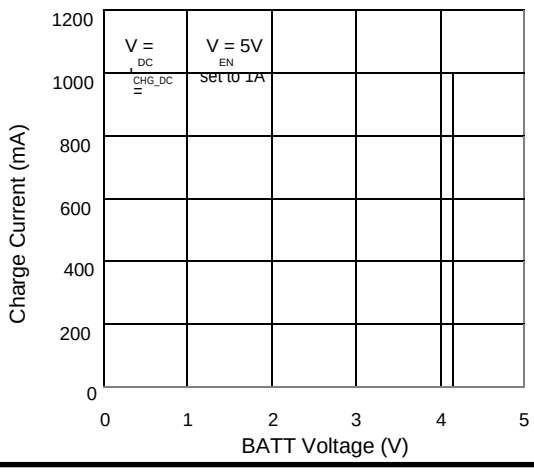
DC Charge Current vs. (V_{DC}-V_{BATT})



USB Charge Current vs. (V_{USB}-V_{BATT})



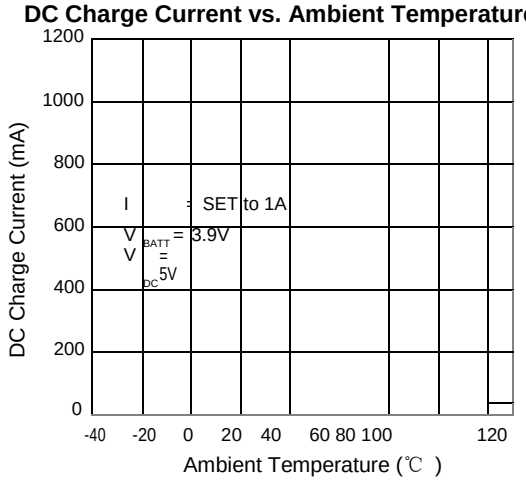
Charge Current vs. BATT Voltage



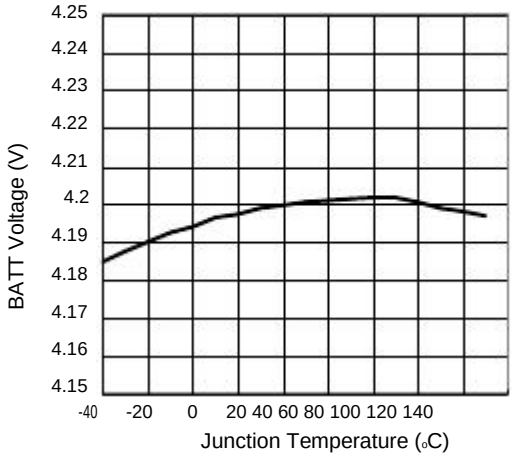
Typical Operating Characteristics (Cont.)

(V_{USB}=V_{DC}=V_{DCLV}=V_{EN}=5V, V_{BATT}=4.2V, V_{THRM}=$V_{REF/2}$, V_{USEL}=5V, Typical Application Circuit 3, T_A=25°C, unless otherwise noted)

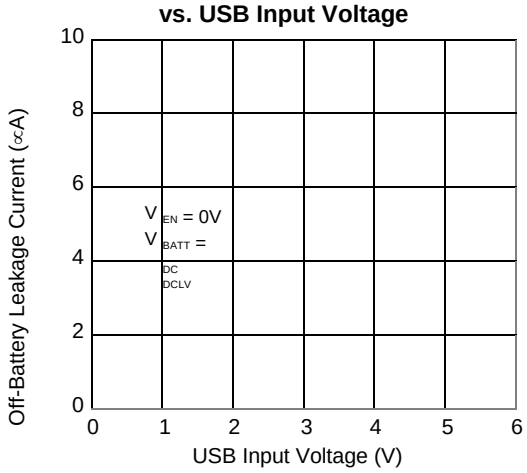
DC Charge Current vs. Ambient Temperature



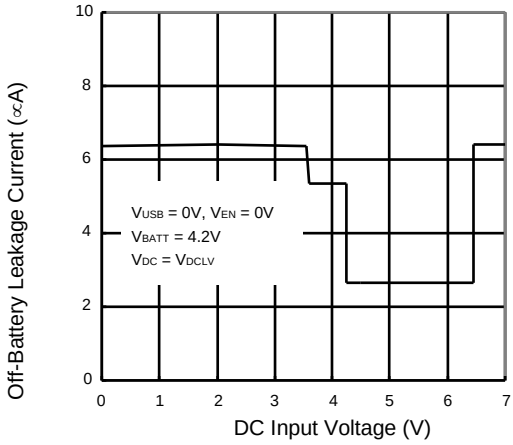
BATT Voltage vs. Junction Temperature



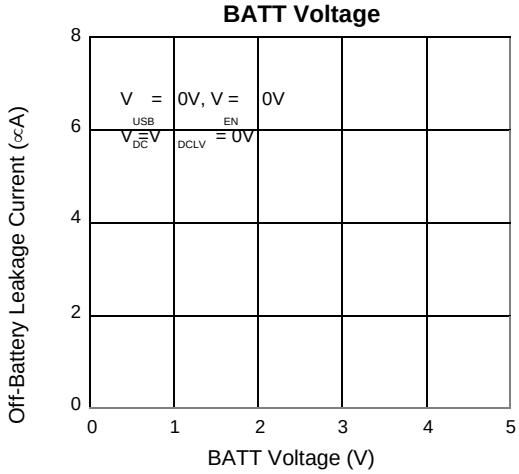
Off-Battery Leakage Current vs. USB Input Voltage



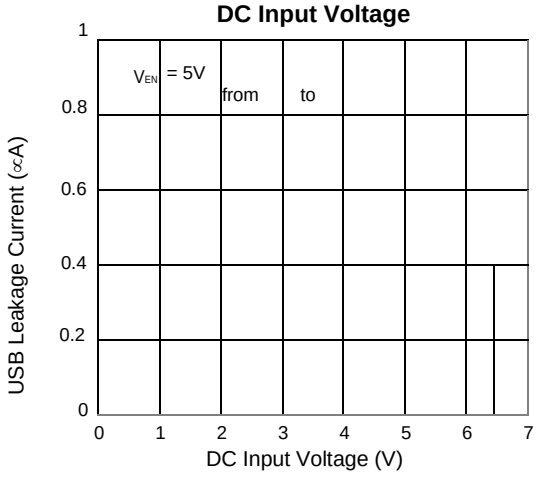
Off-Battery Leakage Current vs. DC Input Voltage



Off-Battery Leakage Current vs. BATT Voltage

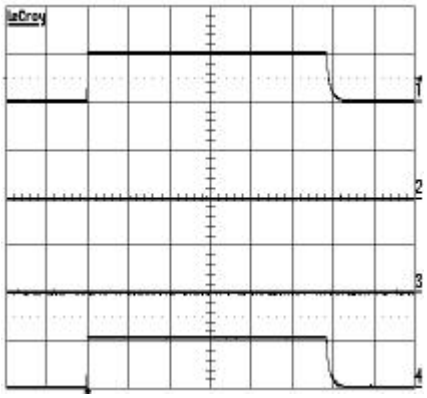


USB Leakage Current vs. DC Input Voltage



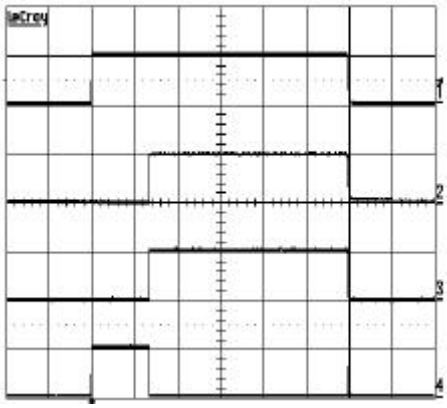
Operating Waveforms

Response to Overvoltage Input



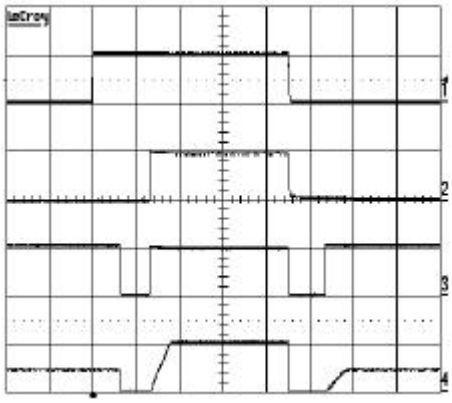
V_{USB}=0V
CH1: V_{DC} (20V/div)
CH2: V_{DCLV} (5V/div)
CH3: V_{PON} (5V/div)
CH4: $V_{\overline{DOCK}}$ (20V/div)
Time: 50ms/div

DC Connect Waveforms



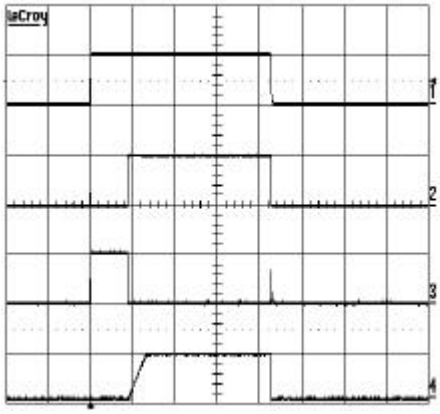
V_{USB} =0V, V_{BATT}=3.9V
CH1: V_{DC} (5V/div)
CH2: V_{DCLV} (5V/div)
CH3: V_{PON} (5V/div)
CH4: $V_{\overline{DOCK}}$ (20V/div)
Time: 20ms/div

DC Connect Waveforms



V_{USB} =5V, V_{BATT}=3.9V
CH1: V_{DC} (5V/div)
CH2: V_{DCLV} (5V/div)
CH3: V_{PON} (5V/div)
CH4: I_{CHG_DC} (1A/div)
Time: 20ms/div

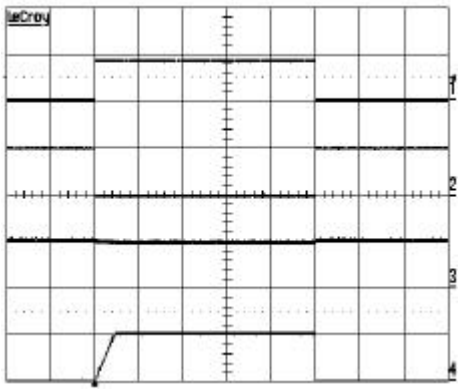
USB Connect Waveforms



V_{DC} =0V, V_{BATT}=3.9V
CH1: V_{USB} (5V/div)
CH2: V_{PON} (5V/div)
CH3: $V_{\overline{UOK}}$ (5V/div)
CH4: I_{CHG_USB} (0.5A/div)
Time: 20ms/div

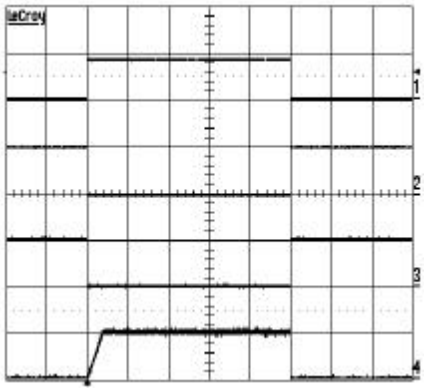
Operating Waveforms (Cont.)

Enable in Fast Charge



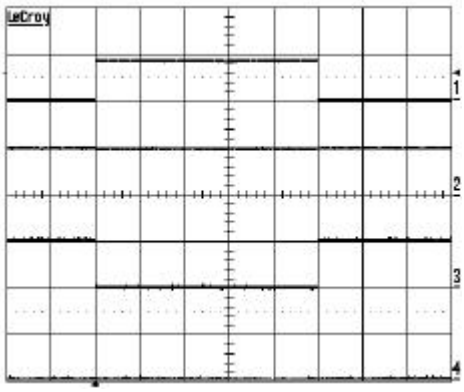
V_{BATT} =3.9V, V_{DC}=5V
CH1: V_{EN} (5V/div)
CH2: V_{STATE1} (5V/div)
CH3: V_{STATE2} (5V/div)
CH4: I_{CHG_DC} (1A/div)
Time: 20ms/div

Enable in Precharge



V_{BATT} =2.7V, V_{DC}=5V
CH1: V_{EN} (5V/div)
CH2: V_{STATE1} (5V/div)
CH3: V_{STATE2} (5V/div)
CH4: I_{CHG_DC} (50mA/div)
Time: 20ms/div

Enable in Charge Done

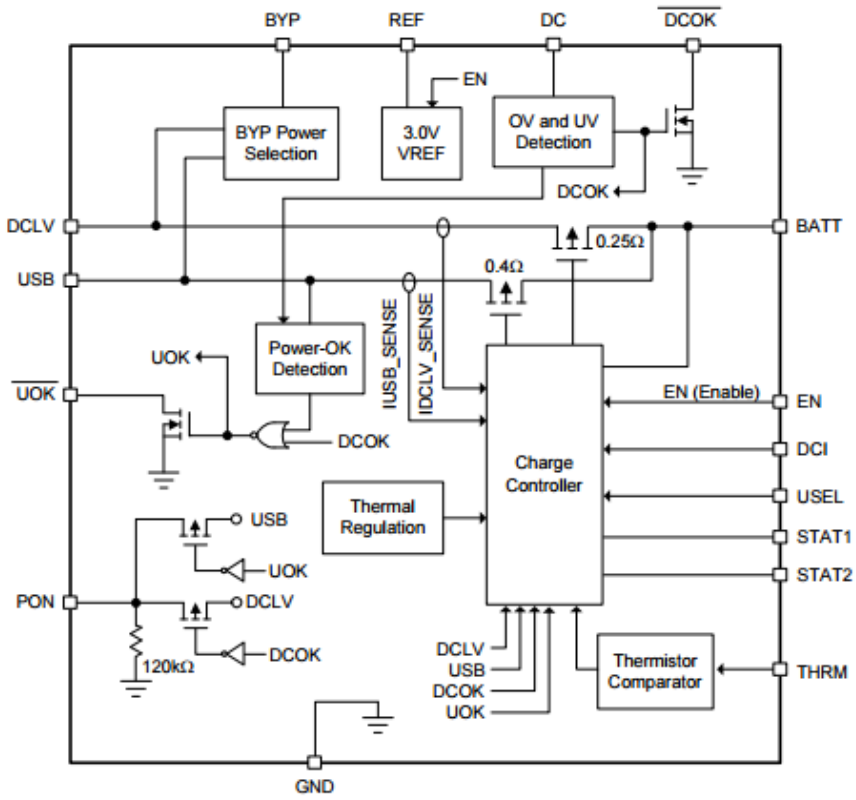


V_{BATT} =4.2V, V_{DC}=5V
CH1: V_{EN} (5V/div)
CH2: V_{STATE1} (5V/div)
CH3: V_{STATE2} (5V/div)
CH4: I_{CHG_DC} (50mA/div)
Time: 20ms/div

Pin Description

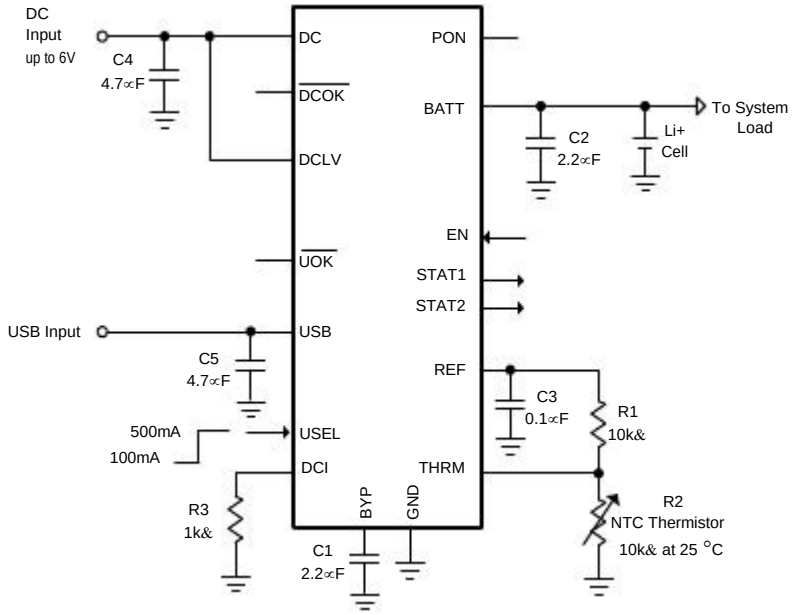
PIN		FUNCTION
NO.	NAME	
1	DCLV	DC charger power input from an AC adapter. DCLV charges BATT through an internal MOSFET. Maximum operating voltage at this pin is 6.0V. When an over-voltage protection MOSFET is connected, DCLV is connected to DC when the input voltage is suitable for
2	DC	Voltage-Sense Pin for DC Input from AC Adapter. Maximum operating voltage at this pin is 18V. This voltage-sense function provides status of DC voltage from AC adapter for over-voltage protection.
3	STAT1	Charge status output pin 1. This pin is an active-high, open-drain output pin.
4	USEL	USB charging current selection input. USEL is a logic input that sets USB source charging current to
5	EN	Charging enable/disable control pin. Drive EN high to enable the device. When EN is low, the charger stops charging and DCOK, UOK, and PON remain active.
6	GND	Signal and power ground.
7	DCI	DC charging current setting pin. Connecting a resistor to the GND sets the fast-charge current when
8	THRM	External thermistor connection pin. THRM pauses charging when an externally connected the thermistor (10k& at +25°C) is at less than 0°C or greater than +50°C. Connecting this pin to the GND disables this function.
9	REF	3V Reference voltage output pin. Sources up to 1.5mA to bias the external thermistor. Bypass with 0.1∝F to the GND. REF loading does not affect BATT regulation accuracy.
10	STAT2	Charge status output pin 2. This pin is an active-high, open-drain output pin.
11	BYP	Bias supply pin for internal circuitry. This pin switches to the pin (either DCLV or USB) with higher supply than the other. Bypass with a 2.2∝F capacitor to the GND.
12	USB	USB charger power input. Charge BATT through an internal MOSFET.
13	UOK	USB power-ok output pin. UOK is an active-low, open-drain output that goes low when USB is the valid charging source (V_{USB} >3.65V and V_{DC}<3.65V).
14	PON	Gate driver output pin for the P-channel MOSFET disconnecting battery from system load when power is applied. PON is an active-high, open-drain output with an internal 140k& resistor to the ground that goes high when V_{DC} or V_{USB} is ready.
15	BATT	Charger output pin. Connect this pin to the positive terminal of a Li+ battery.
16	DCOK	DC power-ok output pin. DCOK is an active-low, open-drain output that goes low when 3.65V < V_{DC} < 6.4V.
Pad	EP	Exposed metal pad. This pad is connected to the ground. Note this internal connection is a soft-connect, meaning there is no internal metal or bond wire physically connecting the exposed pad to the GND pin. The connection is through the silicon substrate of the die and then through a conductive epoxy. Connecting the exposed pad to the ground does not remove the requirement for

Block Diagram



Typical Application Circuits

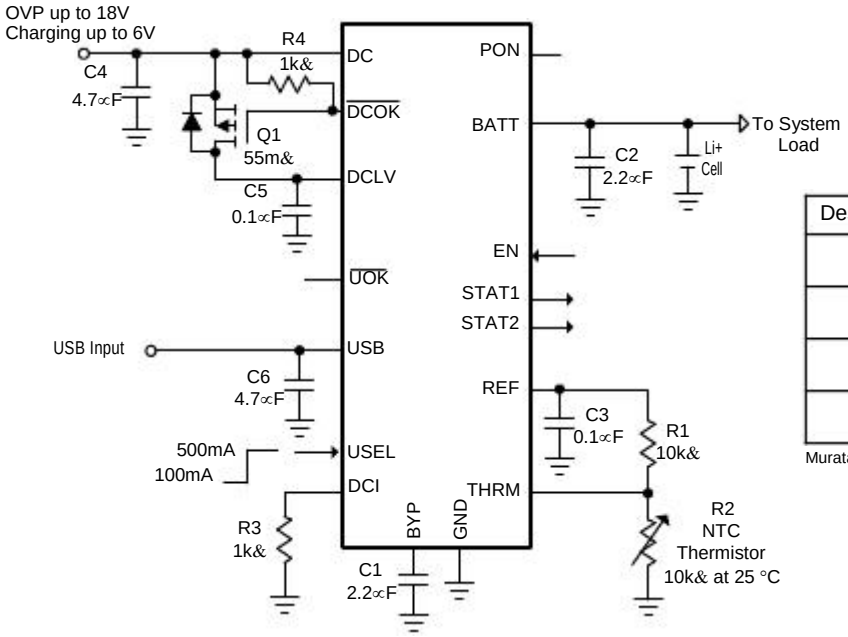
1. A Minimal Circuit that Assumes System Load Is Only Connected to the Battery. The circuit has a 6.0V maximum input and disables charging for inputs over 6.4V.



Designation	Description
C1	2.2∝F, 10V, X5R, 0603 Murata GRM188R61A225K
C2	2.2∝F, 6.3V, X5R, 0603 Murata GRM188R60J225K
C4	4.7∝F, 10V, X5R, 0603 Murata GRM188R61A475K
C5	4.7∝F, 10V, X5R, 0603 Murata GRM188R61A475K

Murata website: www.murata.com

2. A circuit with overvoltage protection MOSFET (Q1) on DC input withstands up to 18V from the AC adapter and disables charging at inputs over 6.4V.

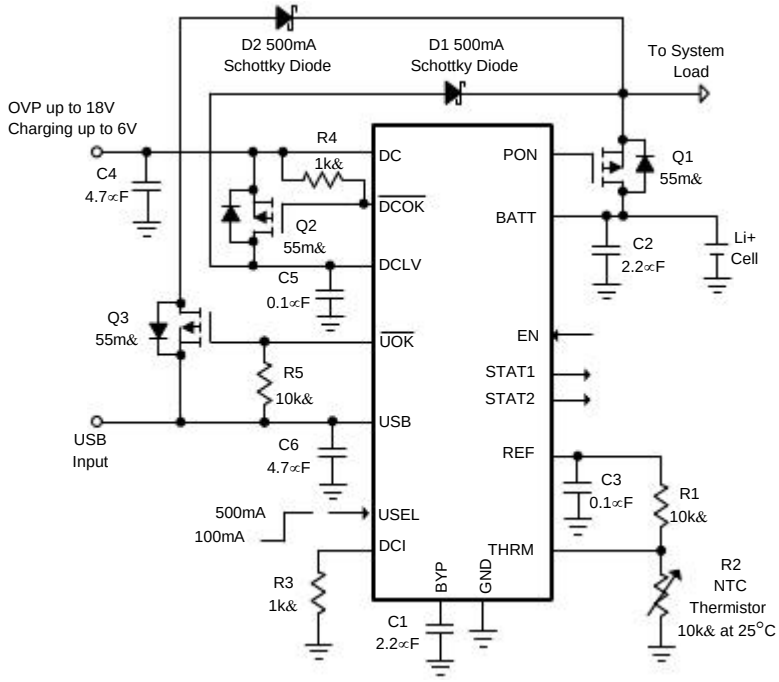


Designation	Description
C1	2.2∝F, 10V, X5R, 0603 Murata GRM188R61A225K
C2	2.2∝F, 6.3V, X5R, 0603 Murata GRM188R60J225K
C4	4.7∝F, 25V, X5R, 0805 Murata GRM21BR61E475K
C6	4.7∝F, 10V, X5R, 0603 Murata GRM188R61A475K

Murata website: www.murata.com

Typical Application Circuits (Cont.)

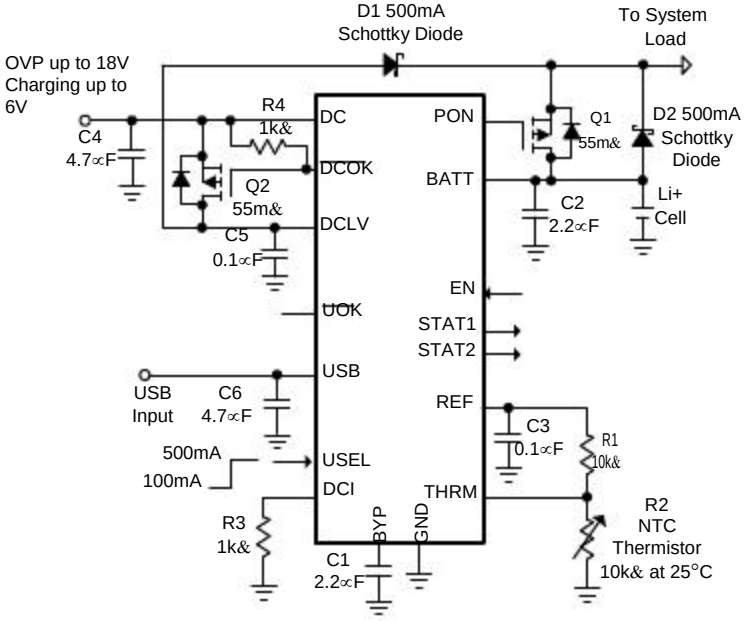
3. Full-Featured Circuit. Overvoltage protection MOSFET (Q2) on DC withstands up to 18V from the AC adapter, but disables charging at inputs over 6.4V. Output switch-over MOSFET (Q1) disconnects the battery from the system load when input power is applied. The input can power the system through D1, D2, Q2, and Q3 when either USB or AC power is present.



Designation	Description
C1	2.2∝F, 10V, X5R, 0603 Murata GRM188R61A225K
C2	2.2∝F, 6.3V, X5R, 0603 Murata GRM188R60J225K
C4	4.7∝F, 25V, X5R, 0805 Murata GRM21BR61E475K
C6	4.7∝F, 10V, X5R, 0603 Murata GRM188R61A475K

Murata website: www.murata.com

4. Partial-Battery Load Switching. AC adapter power is routed directly to system load, but USB power is not. When USB power is connected, total USB current is limited to that set by USEL and system power is drawn from the battery through D2.



Designation	Description
C1	2.2∝F, 10V, X5R, 0603 Murata GRM188R61A225K
C2	2.2∝F, 6.3V, X5R, 0603 Murata GRM188R60J225K
C4	4.7∝F, 25V, X5R, 0805 Murata GRM21BR61E475K
C6	4.7∝F, 10V, X5R, 0603 Murata GRM188R61A475K

Murata website: www.murata.com

Function Description

Autonomous Power Source Selection

The JTMA3200 charges a single-cell Li+ battery from either USB power sources or AC adapter sources. The JTMA3200 includes voltage sensing, monitoring the voltage on the DC pin, and switchover circuitry that selects the active input source to supply charging current. When both inputs are active, priority is given to the AC adapter. Table 1 describes the switchover between AC adaptor and USB power sources.

Table 1 USB and DC Input Selection

DC	USB	Description
V_{DC}>18V	V_{USB}<6.5V	Exceeds operating input range. Not allowed.
V_{DC}<18V	V_{USB}>6.5V	
4V<V_{DC}<6.4V	V_{USB}<6.5V	DCLV supplies charging current.
V_{DC} <4V or V_{DC} >6.4V	V_{USB}>4V	USB supplies charging current.
V_{DC} <4V or V_{DC} >6.4V	V_{USB}<4V	No charging.

When power is connected to DC, the JTMA3200 requires 20ms to validate the input. Consequently, charging is interrupted for 20ms until it is determined that input power is good. Also, when DC power is removed while valid USB power is present, charging is interrupted for 20ms before transferring to the USB source.

An additional power selection circuit selects one of the power sources for control circutry of JTMA3200. The higher voltage on either DCLV or USB supplies control circutry with bias current through the selected internal MOSFET connected from DCLV or USB to BYP. BYP is the bypass connection for the JTMA3200's internal power rail. Bypass to the GND with a 2.2∝F or greater capacitor to reduce voltage ripple.

Enable (EN)

The enable input, EN, switches the charging of JTMA3200 on or off. With EN high, the JTMA3200 can begin charging. When EN is low, $\overline{DCOK}$ and PON remain active. Charging stops when EN is low, but the chip remains biased and continues to draw current from the input supplies. Therefore, power-monitoring outputs can remain valid.

DC Power-OK ($\overline{DCOK}$)

$\overline{DCOK}$ is an active-low and open-drain output that goes low when V_{DC} is below 6.4V and above 3.65V. $\overline{DCOK}$ can be used as a logic output or to drive an external P-channel MOSFET. This allows the charger to protect the input from over-voltage up to 18V. Charging from AC adaptor is disabled for inputs over 6.4V. An external 1k& pull-up resistor keeps $\overline{DCOK}$ high (external MOSFET off) until it is the certain voltage within the acceptable range. To verify that the input voltage is stable, $\overline{DCOK}$ has an internal delay of 20ms before connecting power to DCLV. $\overline{DCOK}$ remains operational when EN is low (charger off).

USB Power-OK ($\overline{UOK}$)

$\overline{UOK}$ is an active-low and open-drain output that goes low to indicate that V_{USB} is valid (greater than 3.65V). $\overline{UOK}$ remains operational when EN is low (charger off). An external 10k& pullup resistor keeps $\overline{UOK}$ high until it is certain that power is within the acceptable range for 20ms. $\overline{UOK}$ can be used as a logic output, or to control a MOSFET that switches USB power directly to the system load when the JTMA3200 is powered from a USB source.

Power On (PON)

PON goes high when V_{DC} or V_{USB} is within its normal operating range(3.65V<V_{DC}<6.4V or V_{USB}>3.65V) to turn off the external P-channel MOSFET, disconnecting the battery from system load. Also, PON can be used as a logic output to indicate power is connected.

The PON has an internal 10& MOSFET for pulling up to BYP voltage and an internal 120k& resistor for pulling down to the GND.

Precharge Current

When the JTMA3200 is powered with a battery connected, the IC first detects if the cell voltage is ready for full charge current. If the cell voltage is less than the prequal level (3V typ.), the battery is precharged with a 50mA current until the cell reaches the proper level. The full charging current, as set by USEL or DCI, is then applied.

Function Description (Cont.)

USB Charging Current

The charging current from the USB source is selected by USEL. A USB source can supply a maximum of 100mA or 500mA. USB hosts and powered hubs typically supply 500mA while unpowered hubs supply 100mA. A logic low on USEL selects a 100mA maximum charging current. A logic high on USEL selects a 500mA maximum charging current.

DC Charging Current

When charging from the DCLV input, the DCI voltage (V_{SET}) and the resistor (R_{SET}) connected from this pin to the GND set the charging current (I_{CHG_DC}) as the following equation :

$$I_{CHG\_DC} = K_{SET} \times \frac{V_{SET}}{R_{SET}}$$

The charging current set factor (K_{SET}) is shown in the Electricl Characteristics. The DCI regulation voltage is reduced by thermal regulation function. Connecting DCI to the GND results in a limited 1.8A charging current.

Battery Full Indication

The JTMA3200 reports the charge-done status on STAT1 and STAT2 pins when the charging current falls below a percentage of the set fast-charge current (Table 2) and the charger is in voltage mode (V_{BATT} near 4.2V).

Table 2 Battery Full Indication

CHARGING SOURCE	CHARGE-DONE CURRENT THRESHOLD
DCLV Charging	12.5% of Fast-charge current and charger in voltage mode
USB Charging (500mA, USEL=high)	125mA and charger in voltage mode
USB Charging (100mA, USEL=low)	Charger in voltage mode

When charging from a DC source, charge-done occurs when I_{CHG_DC} falls to 12.5% of the current set by R_{SET} and the charger is in voltage mode (V_{BATT} near 4.2V). When charging from a USB source with USEL high, charge-done occurs when I_{CHG_USB} falls to 125mA and the charger is in voltage mode. If the JTMA3200 is charging from a USB source with USEL low, charge-done occurs when the charger enters voltage mode.

After the JTMA3200 enunciates the charge-done signal, it keeps operating in voltage mode without turning off the charger and stopping the safety counter.

Thermal Regulation

On-chip thermal limiting in the JTMA3200 simplifies PC board layout and allows charging rates to be automatically optimized without constraints imposed by worstcase minimum battery voltage, maximum input voltage, and maximum ambient temperature. When the JTMA3200 thermal limit is reached, the charger does not shut down but simply reduces charging current. This allows the board design to be optimized for compact size and typical thermal conditions. The JTMA3200 reduces charging current to keep its die temperature below +120°C. The JTMA3200's QFN package includes a bottom metal plate that reduces thermal resistance between the die and the PC board. The external pad should be soldered to a large ground plane. This helps dissipate power and keeps the die temperature below the thermal limit. The JTMA3200's thermal regulator is set for a +120°C die temperature.

External Thermistor Monitor (THRM)

The JTMA3200 features an internal window comparator to monitor battery pack temperature or ambient temperature with an external negative temperature coefficient thermistor. In typical systems, temperature is monitored to prevent charging at ambient temperature extremes (below 0°C or above +50°C). When the temperature moves outside these limits, charging is stopped. If the V_{THERM} returns to its normal window, charging resumes. Connect THRM to the GND when not using this feature. The THRM block diagram is detailed in Figure 1. Note that the temperature monitor at THRM entirely separates from the on-chip temperature limiting discussed in the Thermal Regulation section. The input thresholds for the THRM input are 0.74 x V_{REF} for the COLD trip point and 0.29 x V_{REF} for the HOT trip point.

Function Description (Cont.)

External Thermistor Monitor (THRM) (Cont.)

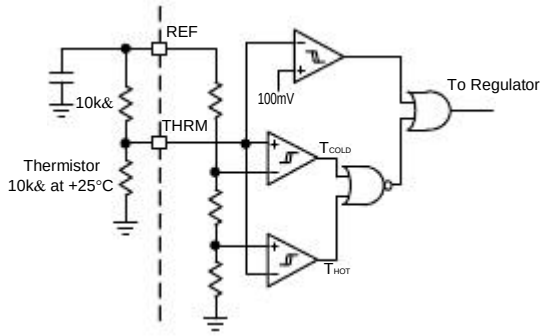


Figure 1. Thermistor Sensing Block Diagram

Sleep Mode

The JTMA3200 charger circuitry enters the low-power sleep mode if both AC adapter and USB power are removed from the circuit. This feature prevents draining the battery into the JTMA3200 during the absence of input supplies. Note that in sleep mode, PON remains low in order for the battery to continue supplying power to the system load.

Table 3 Status Pin Summary

CHARGE STATE	STAT1	STAT2
Precharge in progress	ON	ON
Fast charge in progress	ON	OFF
Charge done	OFF	ON
Charge suspended	OFF	OFF
Sleep mode		

Charge Status Outputs

The open-drain STAT1 and STAT2 outputs indicate various charger operations are shown in Table 3. These status pins can be used to drive LEDs or communicate to the host processor. Note that OFF indicates the open-drain transistor is turned off. Note that this assumes EN=High.

Soft-Start

The JTMA3200 is equipped with a soft-start function to control the rise rate of the charging current rising from zero to the fast-charging current level in constant current mode. During DC charger soft-start, the JTMA3200 ramps up the voltage on DCI pin with constant well-controlled slew rate. The charging current is proportional to the DCI voltage.

The soft-start interval is 7 ms (typical) and is independent of the fast -charging current level.

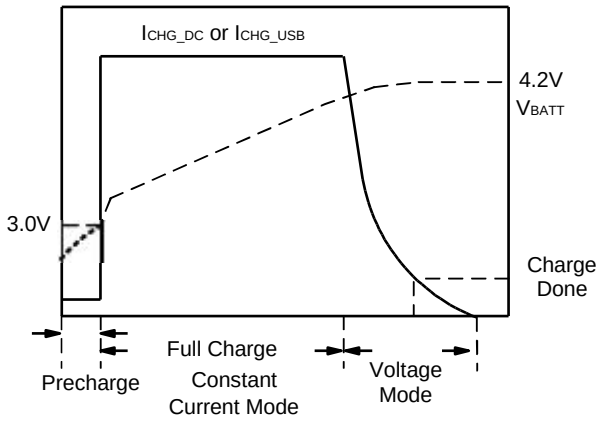


Figure 2. Typical Charging Profile

Applicaiton Information

Input Overvoltage Protection Switch

Connect a P-channel MOSFET between DCLV and DC to protect the DCLV input pin from over-voltage up to 18V. When DC voltage is above 6.4V OVP threshold, the $\overline{DCOK}$ will be pulled high to turn off the P-channel MOSFET. The P-channel MOSFET will be turned on again until the DC voltage is below the OVP threshold. If the OVP function is not needed, leave the $\overline{DCOK}$ open and tie the DC pin to DCLV pin.

Battery-Load Switch

When an AC adapter or USB power is connected to charger, some systems prefer that system load is supplied from the AC adapter or USB power rather than from the battery. In these systems, the battery is permanently connected to system load. If the battery is completely discharged, the system might not ready to operate immediately. If the battery-load switch function is needed, uses external components D1, D2, Q1, Q2, and Q3 to achieve the function.

Typical Application Circuit 3 shows the full-featured circuit. When input power is supplied, the Q1 disconnects the battery from the system load. The input can power the system through D1, D2, Q2, and Q3 when either USB or AC power is present. Typical Application Circuit 4 shows the partial battery-load switching. AC adapter power is routed directly to the battery but USB power is not. When the USB power is connected, total USB current is set by USEL and system power is drawn from the battery through D2.

STAT Pins

The STAT1 and STAT2 outputs indicate various charge status. These two pins can be used to drive LEDs or communicate to the host processor. When status pins are monitored by a processor, there should be a 10k& pull-up resistor to connect each status pin and the V_{CC} of the processor; furthermore, when the status is viewed by LED, the LED with a current rating is less than 10mA and a resistor should be selected to connect LED in series, so the current will be limited to the desired current value. The resistor is calculated by the following equation:

$$R_{LED} = \frac{(V_{IN} - V_{LED\_ON})}{P_D}$$

In other words, the LED and resistor between the input and each status pin shoule in series.

Capacitor Selection

Typically, a 4.7∝F ceramic capacitor is used to connect from DC/USB to the GND. For high charging current, it is recommended to use a larger input bypass capacitance to reduce supply noise. Note that if the OVP function is used, the DC should protect against the high DC input voltage, so the voltage rating of the DC input capacitor must be larger than 25V.

There is a ceramic capacitor connecting from BATT to the GND for proper stability. To work well with most applications, at least a 2.2∝F X5R ceramic capacitor is required.

Thermal Consideration

The JTMA3200 is available in a thermally enhanced QFN package with an exposed pad. It is recommended to connect the exposed pad to a large copper ground plane on the backside of the circuit board through several thermal vias for heatsinking. The exposed pad transfers heat away from the device, allowing the JTMA3200 to charge the battery with maximum current while minimizing the increase in die temperature.

The most common measure of package thermal performance is thermal resistance measured from the device junction to the air surrounding the package surface (θ_{JA}).

The θ_{JA} can be calculated by the following equation:

$$\theta_{JA} = \frac{T_J - T_A}{P_D}$$

where:

T_J=device junction temperature

T_A= ambient temperature

P_D=device power dissipation

The device power dissipation, P_D, is the function of the charge rate and the voltage drop across the internal FET. It can be calculated by the following equation:

Applicaiton Information (Cont.)

Thermal Consideration (Cont.)

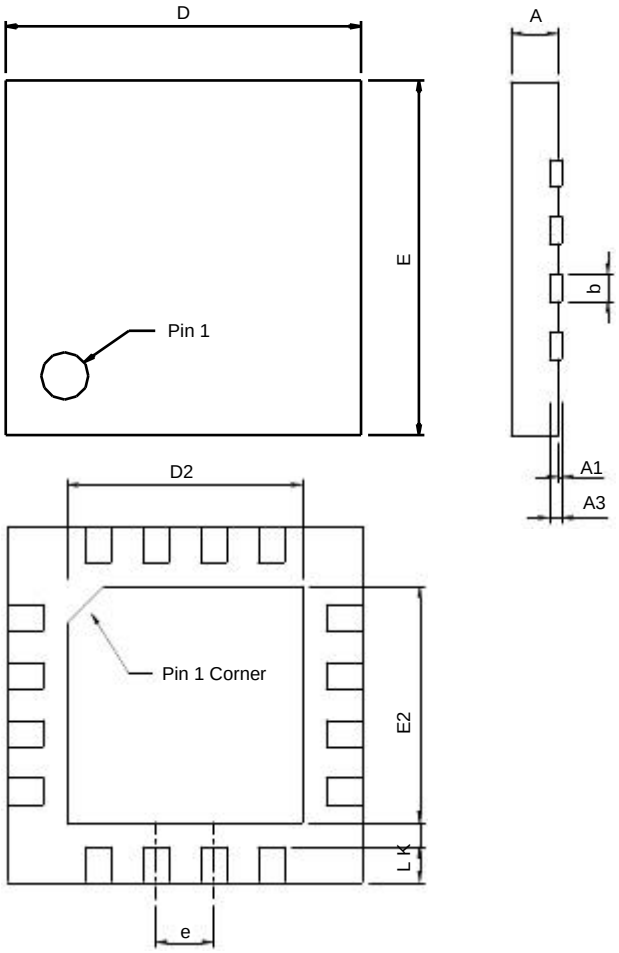
$$P_D=(V_{DCLV}-V_{BATT}) \times I_{CHG\_DC} \text{ (or } I_{CHG\_USB})$$

PCB Layout Consideration

The JTMA3200 is packaged in a thermally enhanced QFN package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed circuit board. Connecting the exposed pad to a large copper ground plane on the backside of the circuit board through several thermal vias for heatsinking is recommended. Connecting the battery to BATT as close to the device as possible provides accurate battery voltage sensing. All decoupling capacitors and filter capacitors should be placed as close as possible to the device. The high-current charge paths into DC, DCLV, USB, and from the BATT pins must short and wide to minimize voltage drops.

Package Information

QFN5x5-16

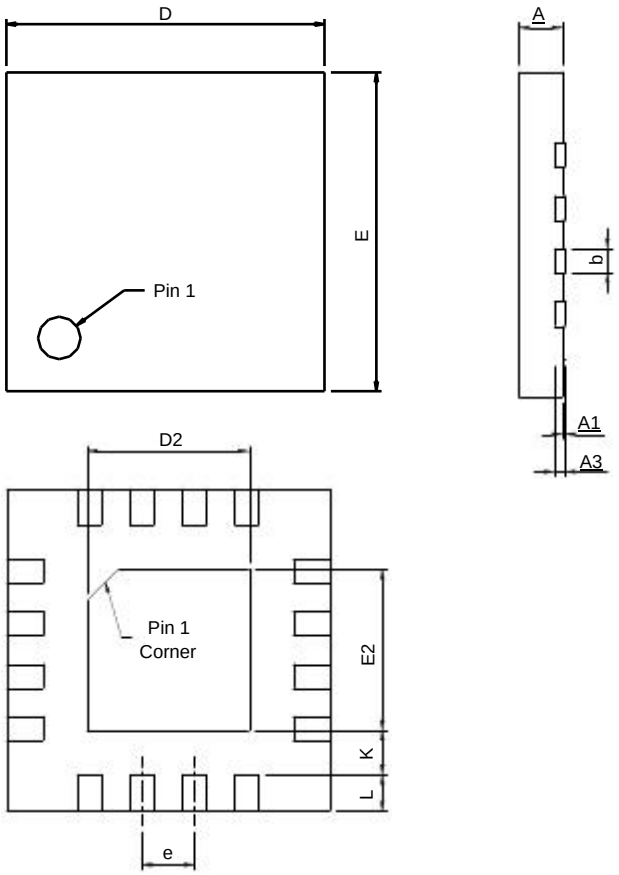


SYMBOL	QFN5x5-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.25	0.35	0.010	0.014
D	4.90	5.10	0.193	0.201
D2	3.10	3.60	0.122	0.142
E	4.90	5.10	0.193	0.201
E2	3.10	3.60	0.122	0.142
e	0.80 BSC		0.031 BSC	
L	0.35	0.60	0.014	0.024
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-220 VHHB.

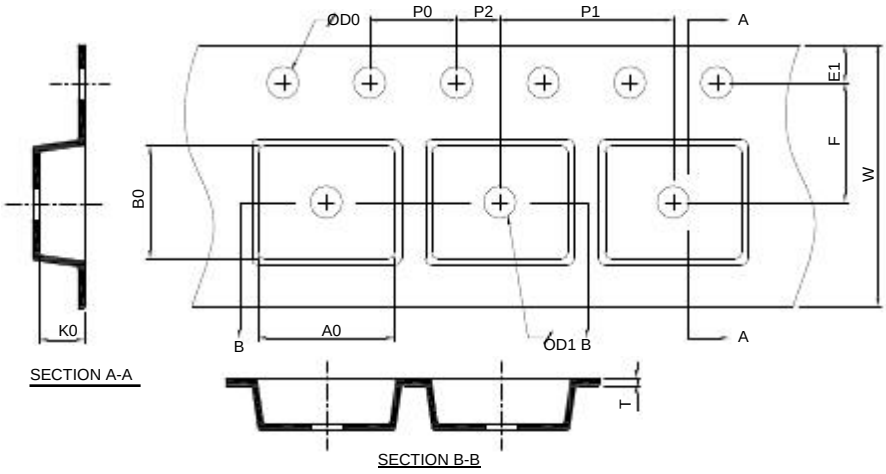
Package Information

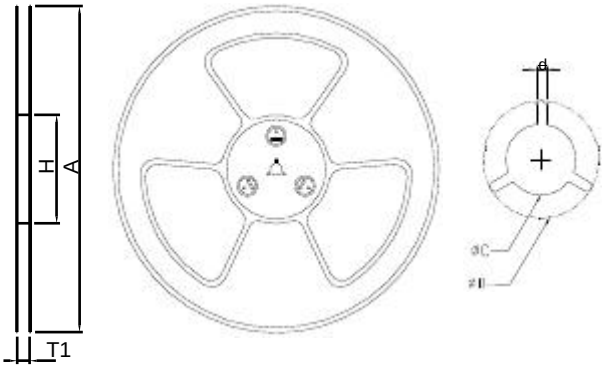
TQFN4x4-16



SYMBOL	TQFN4x4-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.25	0.35	0.010	0.014
D	3.90	4.10	0.154	0.161
D2	1.90	2.10	0.075	0.083
E	3.90	4.10	0.154	0.161
E2	1.90	2.10	0.075	0.083
e	0.65 BSC		0.026 BSC	
L	0.40	0.50	0.016	0.020
K	0.20		0.008	

Carrier Tape & Reel Dimensions





Application	A	H	T1	C	d	D	W	E1	F
QFN5x5-16	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.35±0.20	5.35±0.20	1.30±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TQFN4x4-16	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.30±0.20

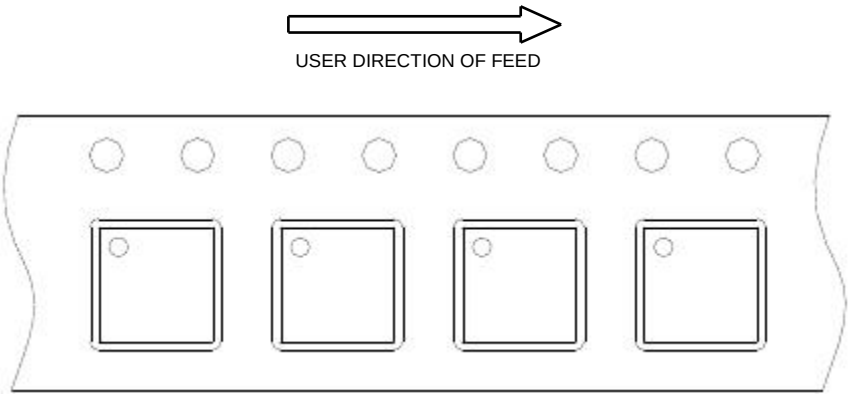
(mm)

Devices Per Unit

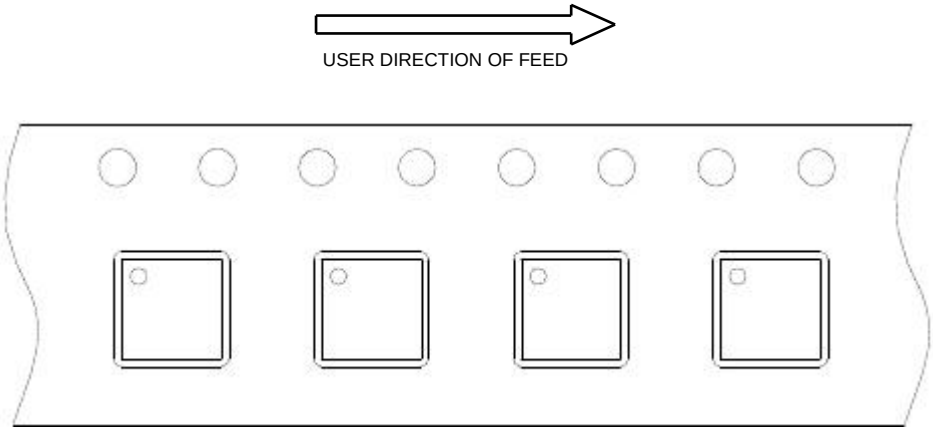
Package Type	Unit	Quantity
QFN5x5-16	Tape & Reel	2500
TQFN4x4-16	Tape & Reel	3000

Taping Direction Information

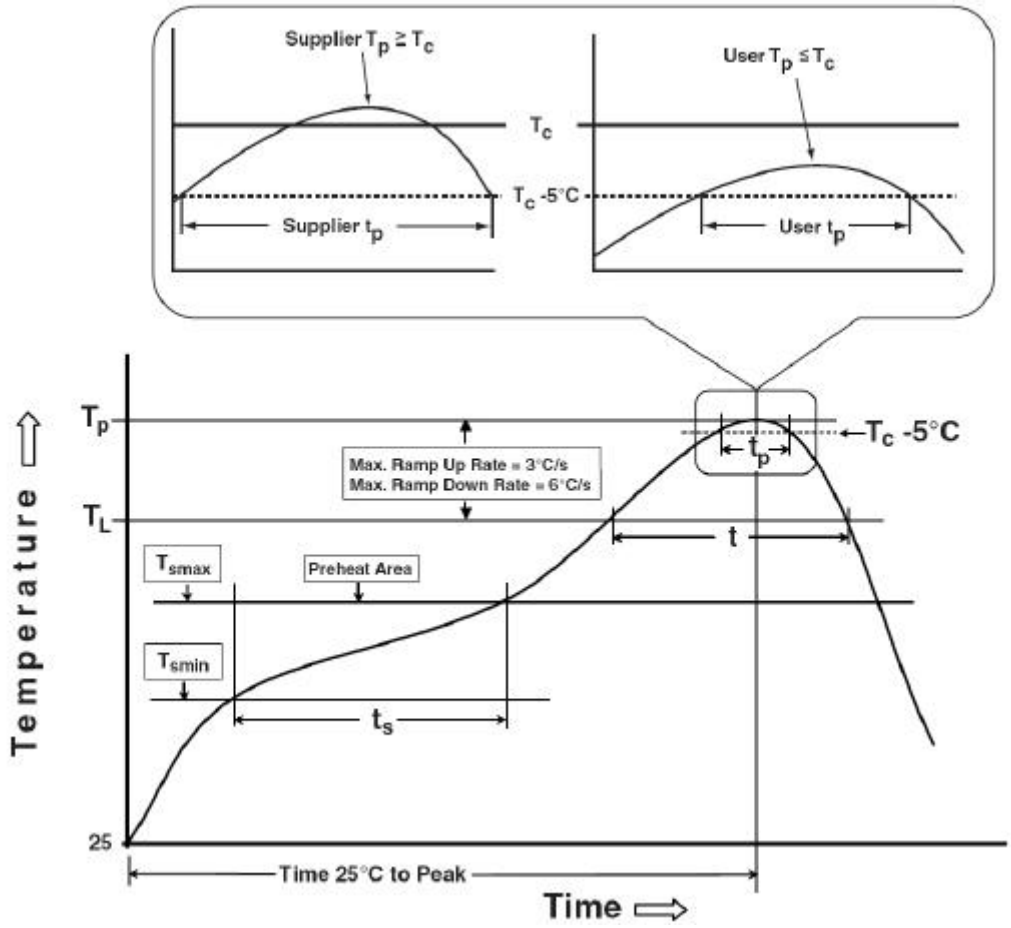
QFN5x5-16



TQFN4x4-16



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ε350
<2.5 mm	235 °C	220 °C
ε2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
ε2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
ESD	MIL-STD-883-3015.7	VHBM≧2KV, VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

Customer Service