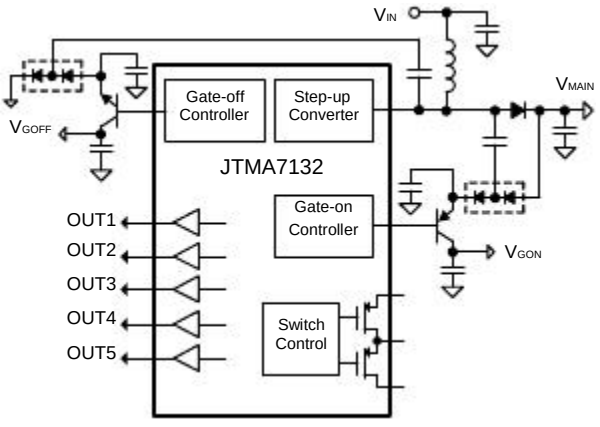
JTMA7130/1/2

TFT-LCD DC-DC Converter With Operational Amplifiers

Features

- **2.6V to 6.5V Input Supply Range**
- **Current-Mode Step-Up Regulator**
  - **Fast Transient Response**
  - **1.2MHz Fixed Operating Frequency**
- **±1.5% High-Accuracy Output Voltage**
- **3A, 20V, 0.25& Internal N-Channel MOSFET**
- **High Efficiency**
- **Low Quiescent Current (0.6mA Typical)**
- **Linear-Regulator Controllers for V_{GON} and V_{GOFF}**
- **High-performance Operational Amplifiers**
  - **±150mA Output Short-Circuit Current**
  - **13V/∝s Slew Rate**
  - **10MHz, -3dB Bandwidth**
  - **Rail-to-Rail Inputs/Outputs**
- **Fault-Delay Timer and Fault Latch for All Regulator Outputs**
- **Over-Temperature Protection**
- **Available in Compact 32-pin 5mmx5mm Thin QFN Package (TQFN5x5-32)**
- **Lead Free Available (RoHS Compliant)**

Simplified Application Circuit



General Description

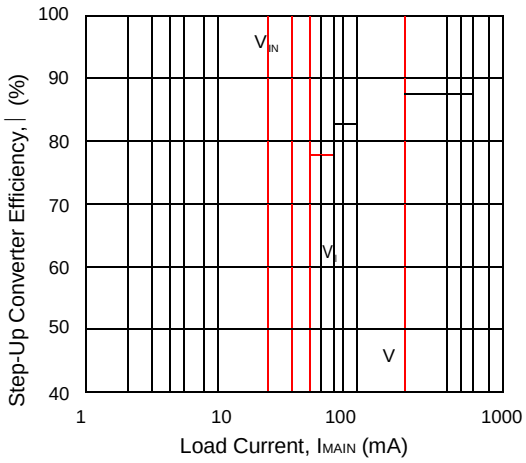
The JTMA71301/2 integrates with a high-performance step-up converter, two linear-regulator controllers, a high voltage switch and one (JTMA7130), three (JTMA7131) or five (JTMA7132) high current operational amplifiers for TFT-LCD applications.

The main step-up regulator is a current-mode, fixed-frequency PWM switching regulator. The 1.2MHz switching frequency allows the usage of low-profile inductors and ceramic capacitors to minimize the thickness of LCD panel designs.

The linear-regulator controllers used external transistors provide regulated the gate-driver of TFT-LCD V_{GON} and V_{GOFF} supplies.

The amplifiers are ideal for VCOM and VGAMMA applications, with 150m A peak output current drive, 10MHz bandwidth, and 13V/μs slew rate. All inputs and outputs are rail-to-rail.

The JTMA7130/1/2 is available in a tiny 5mm x 5mm 32-pin QFN package (TQFN5x5-32).

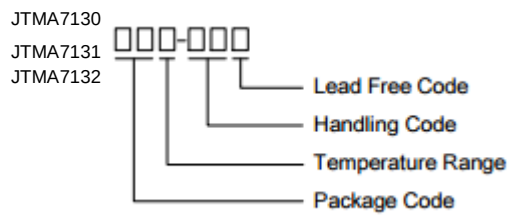


Applications

- **TFT LCD Displays for Monitors**
- **TFT LCD Displays for Notebook Computers**
- **Automotive Displays**

JIATAIMU reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

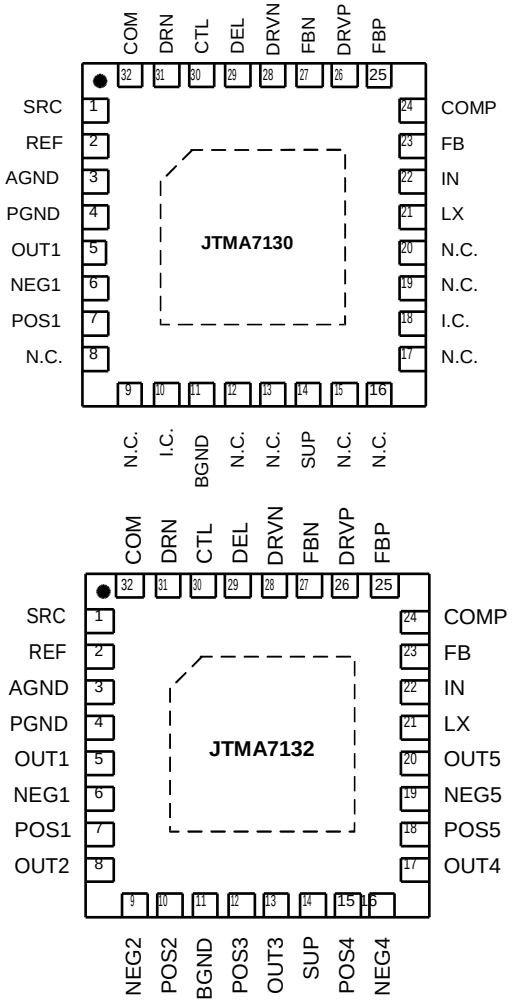


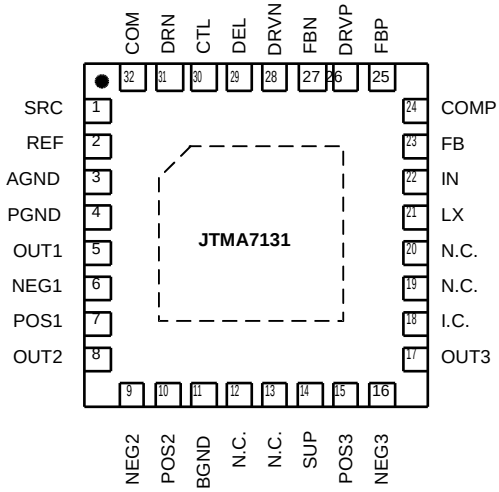
Package Code
QB : TQFN5x5-32
Operating Ambient Temperature Range
I : -40 to 85 C°
Handling Code
TR : Tape & Reel
Lead Free Code
L : Lead Free Device

JTMA7130 QB:	JTMA7130 XXXXX	JTMA7131 QB:	JTMA7131 XXXXX	JTMA7132 QB:	JTMA7132 XXXXX	XXXXX - Date Code

Note: JIATAIMU lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldering operations. JIATAIMU lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Pin Configuration





Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{IN}	IN Supply Voltage (IN to AGND)		-0.3 ~ 7	V
	CTL to AGND Voltage		-0.3 ~ 7	V
	COMP, FB, FBP, FBN REF, DEL, to AGND Voltage		-0.3 ~ V_{IN} + 0.3	V
	PGND, BGND to AGND Voltage		-0.3 ~ 0.3	V
	LX to PGND Voltage	> 100ns	-0.3 ~ 20	V
		< 100ns	-3 ~ 25	V
	DRVP to AGND Voltage		-0.3 ~ 36	V
	DRVN to AGND Voltage		V_{IN} - 25 ~ V_{IN} + 0.3	V
V_{SUP}	SUP to AGND Voltage		-0.3 ~ 20	V
	POS_, NEG_, OUT_ to AGND Voltage		-0.3 ~ V_{SUP} + 0.3	V
	POS1 to NEG1, POS2 to NEG2, POS4 to NEG4, POS5 to NEG5		-6 ~ +6	V
V_{SRC}	SRC to AGND Voltage		-0.3 ~ 36	V
	COM, DRN to AGND Voltage		-0.3 ~ V_{SRC} + 0.3	V
	DRN to COM Voltage		-36 ~ +36	V
	OUT_ Continuous Output Current		-75 ~ +75	mA
	LX Switch Maximum Continuous RMS Output Current		1.6	A
	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds		260	°C

Note 1: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance -Junction to Ambient (Note 2) TQFN5x5-32	43	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of package is soldered directly on the PCB.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	IN Supply Voltage	2.6 ~ 6.5	V
V_{MAIN}	Boost Converter Output Voltage	V_{IN} ~ 18	V
C_{IN}	Boost Converter Input Capacitor	10 ~ 47	∝F
C_{OUT}	Boost Converter Output Capacitor	22 ~ 100	∝F
L_{OUT}	Boost Converter Output Inductor	2.2 ~ 10	∝H
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 100	°C

Note 3: Refer to the application circuit for further information

Electrical Characteristics

Refer to the typical application circuits. These specifications apply over V_{IN} = 5V, I_{OUT} = 0mA, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Condition		APW7130/1/2			Unit
				Min.	Typ.	Max.	
SUPPLY VOLTAGE AND CURRENT							
V_{IN}	IN Supply Voltage Range			2.6	-	6.5	V
I_{IN}	IN Supply Current	V_{FB} = V_{FBP} = 1.4V, V_{FBN} = 0V, LX is not switching		-	0.8	1.0	mA
		V_{FB} = 1.15V, V_{FBP} = 1.4V, V_{FBN} = 0V, LX is switching		-	6	11	
	IN Undervoltage Lockout Threshold	V_{IN} rising		2.25	2.50	2.70	V
	IN Undervoltage Lockout Hysteresis			0.1	0.2	0.3	V
	Duration to Trigger Fault Condition			-	120	-	ms
V_{REF}	REF Output Voltage	-2μA < I_{REF} < 50μA, V_{IN} = 2.6V to 6.5V		1.231	1.250	1.269	V
T_{SD}	Thermal Shutdown Temperature	T_J rising		-	160	-	°C
MAIN STEP-UP REGULATOR							
	Output Voltage Range			V_{IN}	-	18	V
	Operating Frequency			1020	1200	1380	kHz
	Oscillator Maximum Duty Cycle			84	87	90	%
	FB Regulation Voltage	No Load	T_A=+25°C to +85 C°	1.221	1.233	1.245	V
			T_A=0°C to +85 C°	1.218	1.233	1.247	
			T_A=-40°C to +85 C°	1.212	1.233	1.250	
	FB Fault Trip Level	V_{FB} falling		1.1	1.14	1.17	V
	FB Load Regulation	0< I_{MAIN} < full load, Transient Only		-	-1.6	-	%
	FB Line Regulation	V_{IN} = 2.6V to 6.5V		-0.15	+0.04	+0.15	%/V
	FB Input Bias Current	V_{FB} = 1.4V		-40	-	+40	nA
	FB Transconductance	□I_{COMP} = 5μA		75	160	280	μS
	FB Voltage Gain	FB to COMP		-	600	-	V/V
	LX On-Resistance			-	250	500	m&
	LX Leakage Current	V_{LX} = 20V		-	0.02	40	μA
	LX Current-Limit			2.5	3.0	3.5	A
	Current-Sense Transconductance			3.0	3.8	5.0	S
	Soft-Start Period			-	14	-	ms
	Soft-Start Step Size			-	I_{LIM}/8	-	A
OPERATIONAL AMPLIFIERS							
V_{SUP}	SUP Supply Voltage Range			4.5	-	18.0	V
	SUP Supply Current	Buffer configuration, $V_{POS\_}$ = 4V, No Load	APW7132	-	3.3	4.0	mA
			APW7131	-	2.0	2.5	
			APW7130	-	0.7	1.1	
	Input Offset Voltage	Buffer configuration, $V_{POS\_}$=V_{SUP}/2, T_A = 25°C		-	0	12	mV

Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{IN} = 5V, I_{OUT} = 0mA, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Condition	APW7130/1/2			Unit
			Min.	Typ.	Max.	
SUPPLY VOLTAGE AND CURRENT (Cont.)						
	Input Bias Current	($V_{POS\_}$, $V_{NEG\_}$, $V_{OUT\_}$) H V_{SUP}/2	-	+1	+50	nA
	Input Common-Mode Range		0	-	V_{SUP}	V
	Common-Mode Rejection Ratio	0< ($V_{POS\_}$, $V_{NEG\_}$) < V_{SUP}	45	-	-	dB
	Open-Loop Gain		-	125	-	dB
	Output Voltage Swing, High	$I_{OUT\_}$ = 100µA	V_{SUP}-15	V_{SUP}-3	-	mV
		$I_{OUT\_}$ = 5mA	V_{SUP} - 150	V_{SUP} - 80	-	
	Output Voltage Swing, Low	$I_{OUT\_}$ = -100µA	-	2	15	mV
		$I_{OUT\_}$ = -5mA	-	80	150	
	Short-Circuit Current	To V_{SUP}/2, source or sink	100	150	-	mA
	Output Source and Sink Current	($V_{POS\_}$, $V_{NEG\_}$, $V_{OUT\_}$) H V_{SUP}/2, |□V_{OS}| < 10mV (|□V_{OS}| < 30mV for OUT3)	40	-	-	mA
	Power-Supply Rejection Ratio	DC, 6V δ V_{SUP} δ 18V, ($V_{POS\_}$, $V_{NEG\_}$) H V_{SUP}/2	60	-	-	dB
	Slew Rate		-	13	-	V/µs
	-3dB Bandwidth	R_L = 10k&, C_L =10pF, Buffer Configuration	-	10	-	MHz
	Gain Bandwidth Product	Buffer Configuration	-	8	-	MHz
GATE-ON LINEAR REGULATOR CONTROLLER						
	FBP Regulation Voltage	I_{DRVP} = 100µA	1.218	1.250	1.269	V
	FBP Fault Trip Level	V_{FBP} falling	0.96	1.00	1.04	V
	FBP Input Bias Current	V_{FBP} = 1.4V	-50	-	+50	nA
	FBP Effective Load Regulation Error (Transconductance)	V_{DRVP} = 10V, I_{DRVP}=50µA to 1mA	-	-0.7	-1.5	%
	FBP Line (IN) Regulation Error	I_{DRVP} = 100µA, 2.6V < V_{IN} < 6.5V	-	±1.5	±5	mV
	DRVP Sink Current	V_{FBP} = 1.1V, V_{DRVP} = 10V	1	5	-	mA
	DRVP Off-Leakage Current	V_{FBP} = 1.4V, V_{DRVP} = 28V	-	0.01	10	µA
	Soft-Start Period		-	14	-	ms
	Soft-Start Step Size		-	V_{REF}/128	-	V
GATE-OFF LINEAR-REGUALTOR CONTROLLER						
	FBN Regulation Voltage	I_{DRVN} = 100µA	235	250	265	mV
	FBN Fault Trip Level	V_{FBN} rising	370	420	470	mV
	FBN Input Bias Current	V_{FBN} = 0V	-50	-	+50	nA
	FBN Effective Load-Regulation Error (Transconductance)	V_{DRVN} = -10V, I_{DRVN} = 50µA to 1mA	-	11	25	mV
	FBN Line (IN) Regulation Error	I_{DRVN}=100µA, 2.6V< V_{IN} <6.5V	-	±0.7	±5	mV

Electrical Characteristics (Cont.)

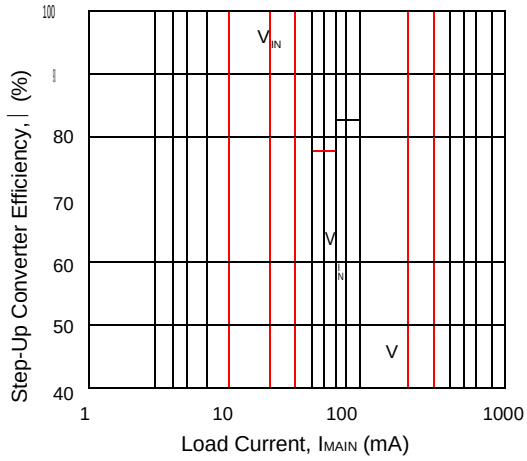
Refer to the typical application circuits. These specifications apply over V_{IN} = 5V, I_{OUT} = 0mA, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Condition	APW7130/1/2			Unit
			Min.	Typ.	Max.	
GATE-OFF LINEAR-REGUALTOR CONTROLLER						
	DRVN Source Current	V_{FBN} = 500mV, V_{DRVN} = -10V	1	4	-	mA
	DRVN Off-Leakage Current	V_{FBN} = 0V, V_{DRVN} = -25V	-	-0.01	-10	μA
	Soft-Start Period		-	14	-	ms
	Soft-Start Step Size		-	V_{REF}/ 128	-	V
POSITIVE GATE-DRIVER TIMING AND CONTROL SWITCHES						
	DEL Capacitor Charge Current	During startup, V_{DEL} = 1V	4	5	6	μA
	DEL Turn-On Threshold		1.19	1.25	1.31	V
	DEL Discharge Switch On-Resistance	During UVLO, V_{IN} = 2.2V	-	33	-	&
	CTL Input Low Voltage	V_{IN} = 2.6V to 6.5V	-	-	0.6	V
	CTL Input High Voltage	V_{IN} = 2.6V to 6.5V	2	-	-	V
	CTL Input Leakage Current	CTL = AGND or IN	-1	-	+1	μA
	CTL-to-SRC Propagation Delay		-	100	-	ns
V_{SRC}	SRC Input Voltage Range		-	-	36	V
	SRC Input Current	V_{DEL} = 1.5V, CTL = IN	-	50	100	μA
		V_{DEL} = 1.5V, CTL = AGND	-	30	50	
	SRC to COM Switch On-Resistance	V_{DEL} = 1.5V, CTL = IN	-	6	12	&
	DRN to COM Switch On-Resistance	V_{DEL} = 1.5V, CTL = AGND	-	35	70	&

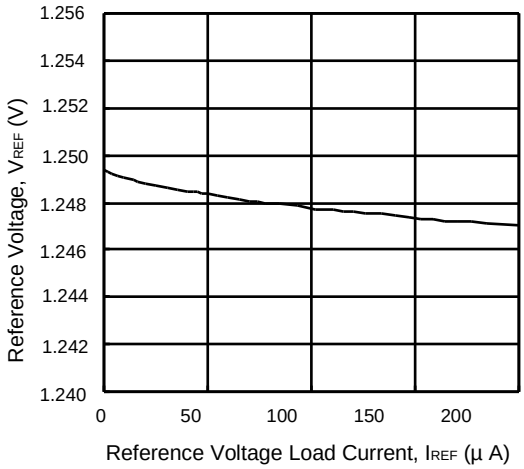
Typical Operating Characteristics

(Refer to Fig 1. in the section “Typical Application Circuits”, V_{IN}=5V, T_A=25°C, unless otherwise specified)

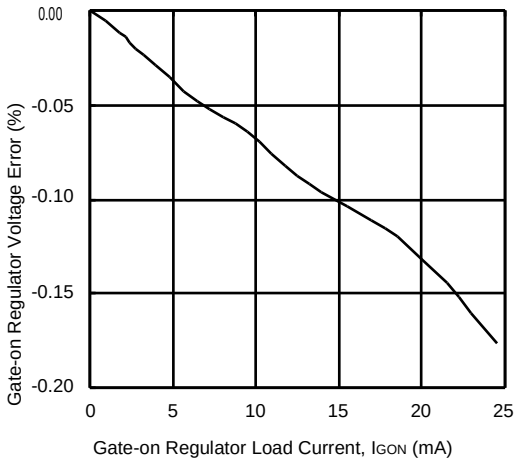
Step-Up Efficiency vs. Load Current



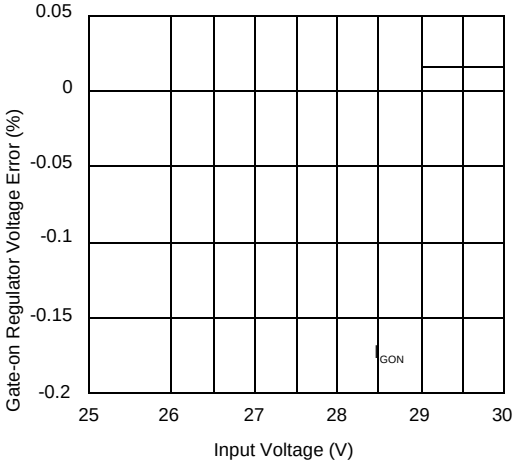
Reference Voltage Load Regulation



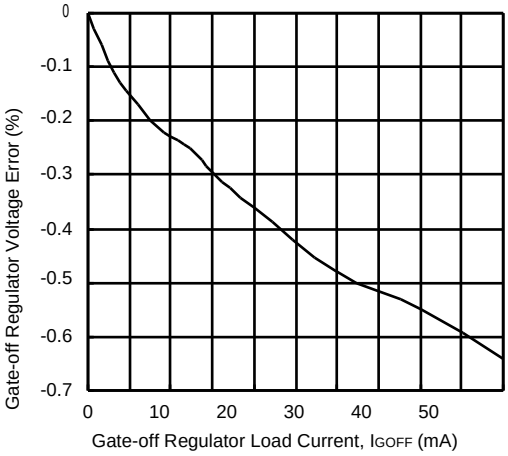
Gate-on Regulator Load Regulation



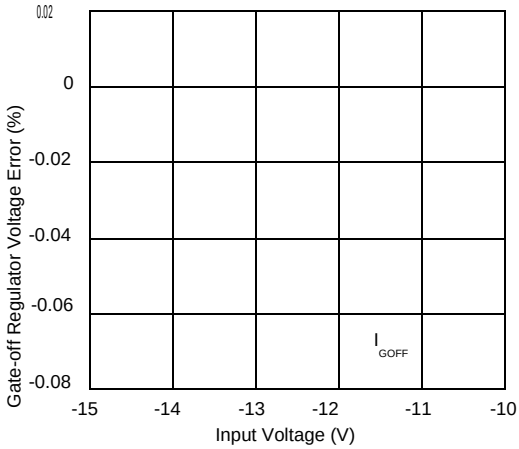
Gate-on Regulator Line Regulation



Gate-off Regulator Load Regulation



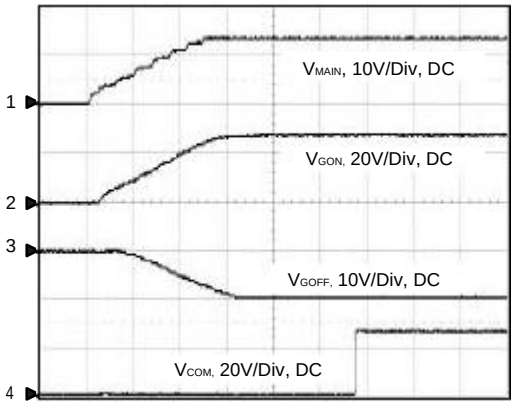
Gate-off Regulator Line Regulation



Operating Waveforms

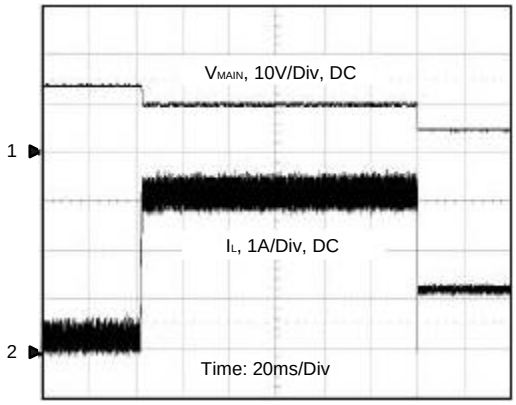
(Refer to Fig 1. in the section “Typical Application Circuits”, V_{IN}=5V, V_{MAIN}=14V, V_{GON}=25V, V_{GOFF}=-10V, T_A=25°C, unless otherwise specified)

Start-Up Sequence



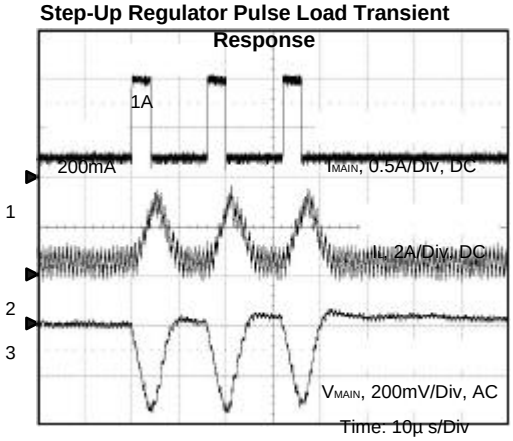
CH1: V_{MAIN}, 10V/Div, DC
CH2: V_{GON}, 20V/Div, DC
CH3: V_{GOFF}, 10V/Div, DC
CH4: V_{COM}, 20V/Div, DC
Time: 5ms/Div

Over Load Protection



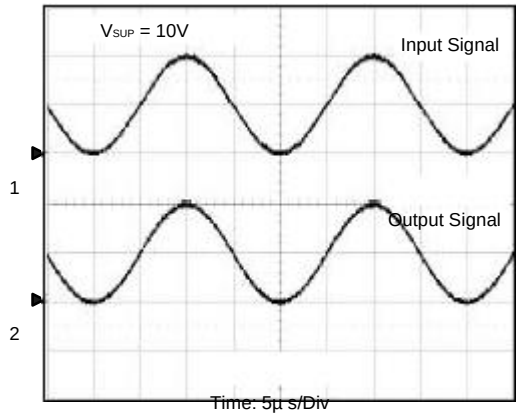
CH1: V_{MAIN}, 10V/Div, DC
CH2: I_{MAIN}, 1A/Div, DC
Time: 20ms/Div

Step-Up Regulator Pulse Load Transient Response



CH1: I_{MAIN}, 0.5A/Div, DC
CH2: I_L, 2A/Div, DC
CH3: V_{MAIN}, 200mV/Div, AC
Time: 10µs/Div

Operational Amplifier Rail to Rail Input/Output



CH1: Input Signal, 5V/Div, DC
CH2: Output Signal, 5V/Div, DC
Time: 5µs/Div

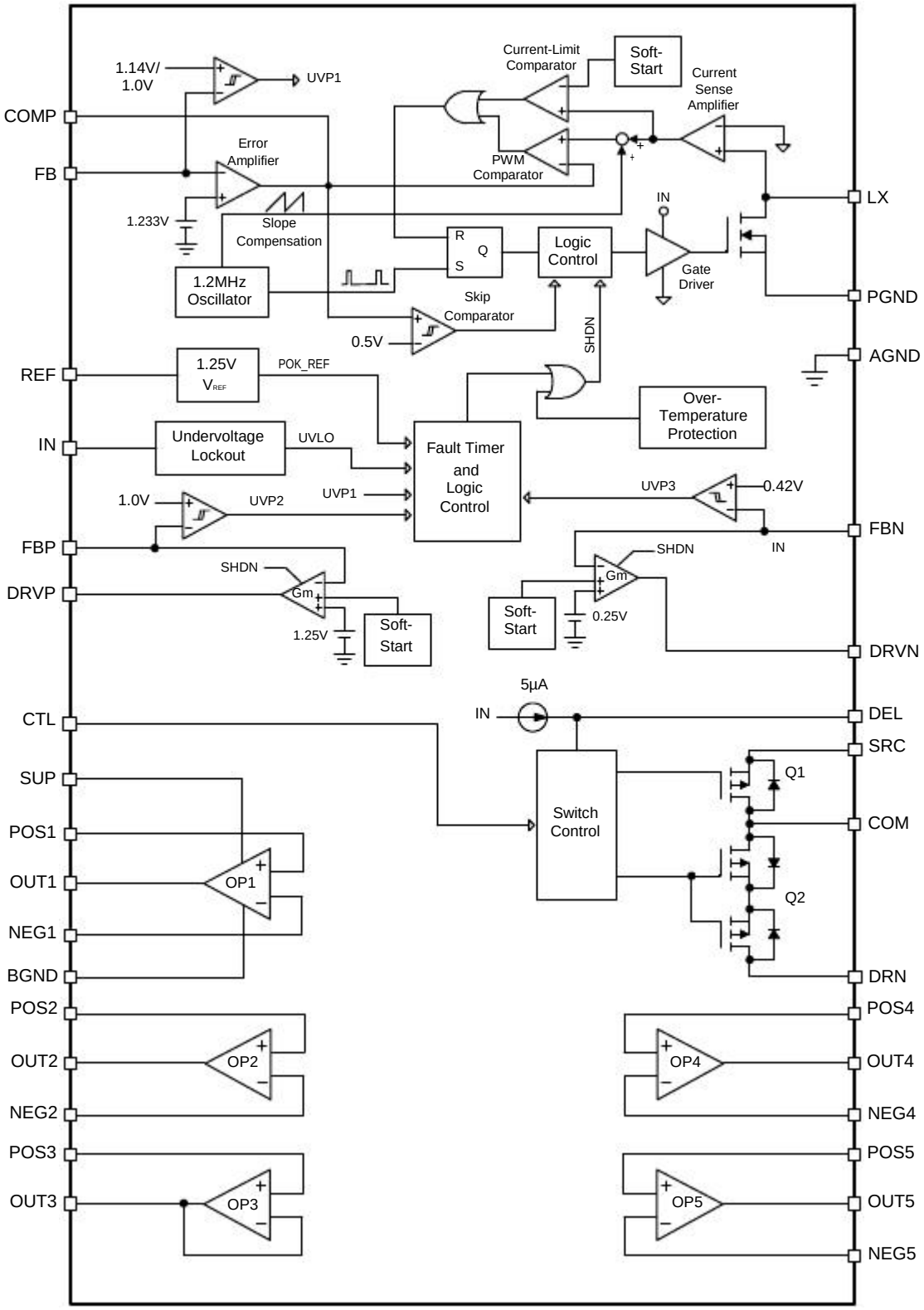
Pin Description

Pin	Name			Function Description
	APW7130	APW7131	APW7132	
1	SRC	SRC	SRC	Switch Input. Source of the internal high-voltage P-channel MOSFET. Bypass SRC to PGND with a minimum of 0.1µF capacitor closed to the pins.
2	REF	REF	REF	Reference voltage output. Bypass REF to AGND with a minimum of 0.22µFcapacitor closed to the pins.
3	AGND	AGND	AGND	Analog Ground for Step-Up Regulator and Linear Regulators. Connect to power ground (PGND) underneath the IC.
4	PGND	PGND	PGND	Power Ground for Step-Up Regulator. PGND is the source of the main step-up n-channel power MOSFET. Connect PGND to the ground terminals of output capacitors through a short, wide PC board trace. Connect to analog ground (AGND) underneath the IC.
5	OUT1	OUT1	OUT1	Output of Operational-Amplifier 1
6	NEG1	NEG1	NEG1	Inverting Input of Operational-Amplifier 1
7	POS1	POS1	POS1	Non-inverting Input of Operational-Amplifier 1
8	NC	OUT2	OUT2	Output of Operational-Amplifier 2 of APW7132/APW7131. No internal connected of APW7130.
9	NC	NEG2	NEG2	Inverting Input of Operational-Amplifier 2 of APW7132/APW7131. No internal connected of APW7130.
10	IC	POS2	POS2	Non-inverting Input of Operational-Amplifier 2 of APW7132/APW7131. Internal connected to GND of APW7130
11	BGND	BGND	BGND	Analog Ground for Operational Amplifiers. Connect to power ground (PGND) underneath the IC.
12	NC	NC	POS3	Non-inverting Input of Operational-Amplifier 3 of APW7132. No internal connected of APW7131/APW7130.
13	NC	NC	OUT3	Output of Operational-Amplifier 3 of APW7132. No internal connected of APW7131/APW7130.
14	SUP	SUP	SUP	Power Input of Operational Amplifiers. Typically connected to V_{MAIN}. Bypass SUP to BGND with a 0.1µF capacitor.
15	NC	POS3	POS4	Non-inverting Input of Operational-Amplifier 4 of APW7132. Non-inverting Input of Operational-Amplifier 3 of APW7131. No internal connected of APW7130.
16	NC	NEG3	NEG4	Inverting Input of Operational-Amplifier 4 of APW7132. Inverting Input of Operational-Amplifier 3 of APW7131. No internal connected of APW7130.
17	NC	OUT3	OUT4	Output of Operational-Amplifier 4 of APW7132. Output of Operational-Amplifier 3 of APW7131. No internal connected of APW7130.
18	IC	IC	POS5	Non-inverting Input of Operational-Amplifier 5 of APW7132. Internal connected to GND of APW7131/APW7130.
19	NC	NC	NEG5	Inverting Input of Operational-Amplifier 5 of APW7132. No internal connected of APW7131/APW7130.
20	NC	NC	OUT5	Output of Operational-Amplifier 5 of APW7132. No internal connected of APW7131/APW7130.
21	LX	LX	LX	N-Channel Power MOSFET Drain and Switching Node. Connect the inductor and Schottky diode to LX and minimize the trace area for lowest EMI.
22	IN	IN	IN	Supply Voltage Input. Bypass IN to AGND with a 0.1µF capacitor. IN can range from 2.6V to 6.5V.
23	FB	FB	FB	Step-Up Regulator Feedback Input. Connect a resistive voltage-divider from the output (V_{MAIN}) to FB to analog ground (AGND). Place the divider within 5mm of FB.
24	COMP	COMP	COMP	Step-Up Regulator Error-Amplifier Compensation Point. Connect a series RC from COMP to AGND.

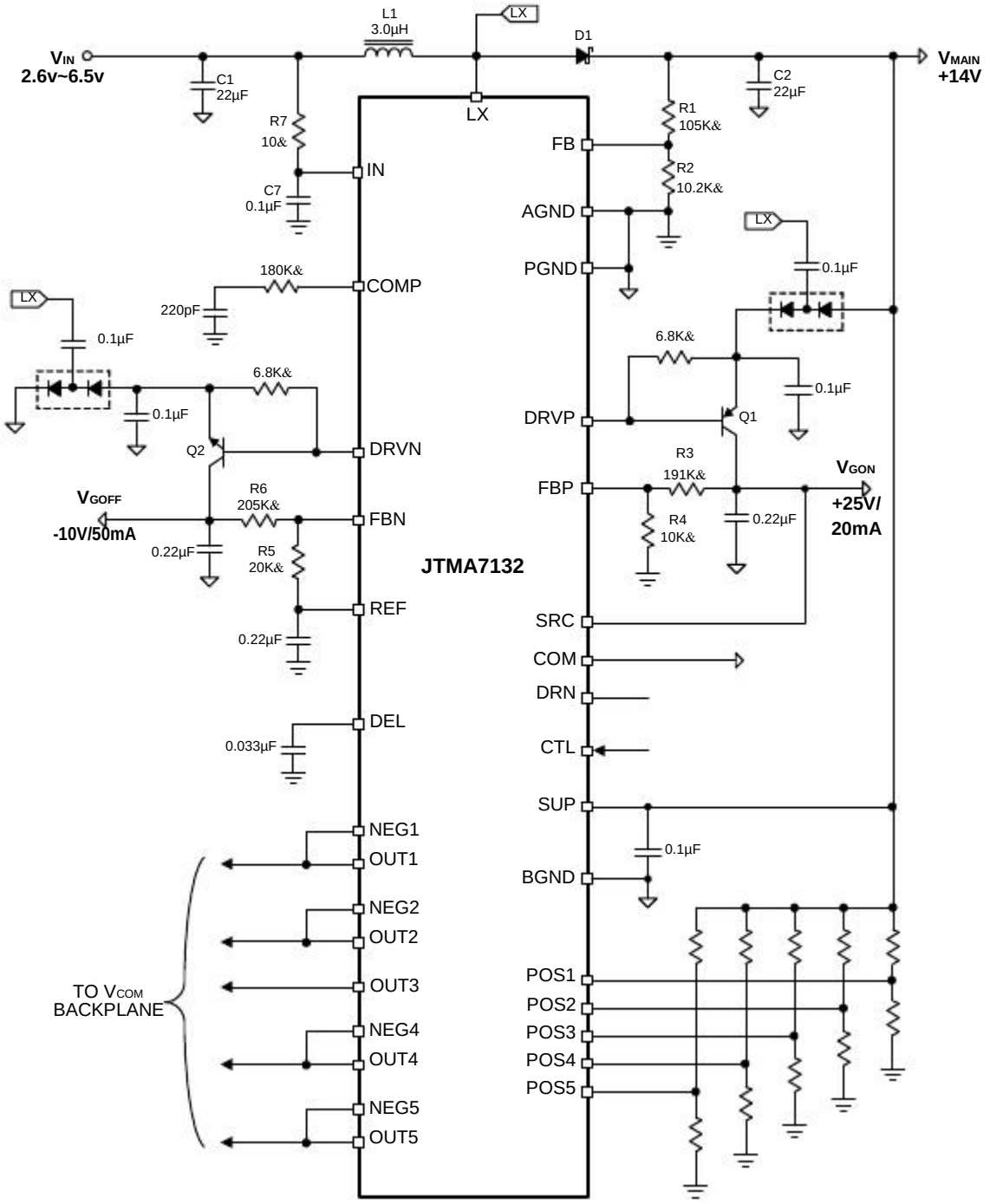
Pin Description (Cont.)

Pin	Name			Function Description
	APW7130	APW7131	APW7132	
24	COMP	COMP	COMP	Step-Up Regulator Error-Amplifier Compensation Point. Connect a series RC from COMP to AGND.
25	FBP	FBP	FBP	Gate-On Linear-Regulator Feedback Input. Connect FBP to the center of a resistive voltage-divider between the regulator output and AGND to set the gate-on linear regulator output voltage. Place the resistive voltage-divider close to the pin.
26	DRVP	DRVP	DRVP	Gate-On Linear-Regulator Base Drive. Open drain of an internal n-channel MOSFET. Connect DRVP to the base of an external PNP pass transistor.
27	FBN	FBN	FBN	Gate-Off Linear-Regulator Feedback Input. Connect FBN to the center of a resistive voltage-divider between the regulator output and REF to set the gate-off linear regulator output voltage. Place the resistive voltage-divider close to the pin.
28	DRVN	DRVN	DRVN	Gate-Off Linear-Regulator Base Drive. Open drain of an internal p-channel MOSFET. Connect DRVN to the base of an external NPN pass transistor.
29	DEL	DEL	DEL	High-Voltage Switch Delay Input. Connect a capacitor from DEL to AGND to set the high-voltage switch startup delay.
30	CTL	CTL	CTL	High-Voltage Switch Control Input. When CTL is high, the high-voltage switch between COM and SRC is on and the high-voltage switch between COM and DRN is off. When CTL is low, the high-voltage switch between COM and SRC is off and the high-voltage switch between COM and DRN is on. CTL is inhibited by the undervoltage lockout and when the voltage on DEL is less than 1.25V.
31	DRN	DRN	DRN	Switch Input. Drain of the internal high-voltage back-to-back P-channel MOSFETs connected to COM. Do not allows the voltage on DRN to exceed V_{SRC}.
32	COM	COM	COM	Internal High-Voltage MOSFET Switch Common Terminal. Do not allow the voltage on COM to exceed V_{SRC}.

Block Diagram



Typical Application Circuits



Function Description

The JTMA7130/1/2 integrates a high performance step-up switching regulator, two linear-regulator controllers, multiple high-current operational amplifiers, and startup timing and level-shifting functionality which is useful for active-matrix TFT-LCD. Figure 2 shows the block diagram.

Main Step-up Regulator

The main step-up regulator is a current-mode and fixed-frequency PWM switching regulator. The 1.2MHz switching frequency allows the usage of low-profile inductors and ceramic capacitors to minimize the thickness of LCD panel designs. The output voltage can be set from V_{IN} to 18V with an external resistive voltage-divider. The regulator can operate under both discontinuous and continuous inductor current mode. Although the regulator is designed to operate under continuous current mode originally, it can also well operate under discontinuous current mode at light load. In continuous current mode, current flows continuously in the inductor during the entire switching cycle in steady state operation. The voltage conversion ratio in continuous current mode is given by:

$$\frac{V_{MAIN}}{V_{IN}} = \frac{1}{1 - D}$$

where D is the duty cycle of switching MOSFET.

Figure 2 shows the block diagram of the step-up regulator. During normal operation, the internal N-channel power MOSFET is turned on in each cycle when the oscillator sets an internal RS latch and is turned off when an internal comparator (ICMP) resets the latch. The peak inductor current at which ICMP resets the RS latch is controlled by the voltage on the COMP pin which is the output of the error amplifier (EAMP). An external resistive divider connected between V_{OUT} and ground allows the EAMP to receive an output feedback voltage (V_{FB}) at FB pin. When the load current increases, it causes slightly decrease in V_{FB} associated with the reference (V_{REF}), which in turn causes the COMP voltage to increase until the average inductor current matches the new load current.

Current-Limit Protection of Step-Up Regulator

The JTMA7130/1/2 monitors the output current, flowing through the P-channel MOSFET, and limits the current peak at current-limit level to prevent loads and the JTMA7130/1/2 from damages during overload or short-circuit conditions.

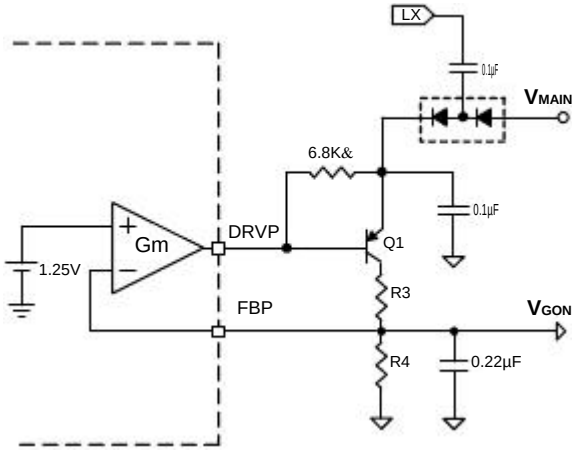


Figure 4. Application Circuit of V_{GON}

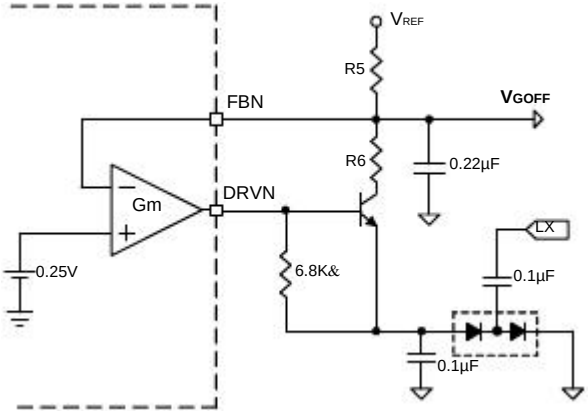


Figure 5. Application Circuit of V_{GOFF}

Linear-Regulator Controller (Gate-On and Gate-Off)

The JTMA7130/1/2 includes 2 independent linear-regulator controllers, in which there is one positive output voltage (V_{GON}), and one negative voltage (V_{GOFF}). The V_{GON} and V_{GOFF} linear-regulator controller block diagram and application circuit are shown in Figure 4 and Figure 5 respectively.

The gate-on linear-regulator is used to provide the positive gate-on voltage (V_{GON}) for the TFT-LCD gate driver. The DC/DC consists of an external diode-capacitor charge pump powered by the inductor (LX) of the step-up converter, followed by a low dropout linear regulator. The linear controller drives an external PNP transistor as the pass element. The internal controller is a wide band transconductance amplifier capable to sink current at least 1mA, which is sufficient to deliver 50mA or more output current. Typically, the JTMA7130/1/2 could support gate-

Function Description (Cont.)

Linear-Regulator Controller (Gate-On and Gate-Off) (Cont.)

on voltage (V_{GON}) ranges from +15V to +36V. A fault comparator is also included for monitoring the output voltage. The undervoltage threshold is set at 110mV below the 1.25V reference level.

The gate-off linear-regulator is used to provide the negative gate-off voltage (V_{GOFF}) for the TFT-LCD gate driver. The DC/DC consists of an external diode-capacitor charge pump powered by the inductor (LX) of the step-up converter, followed by a low dropout linear regulator. The linear controller drives an external NPN transistor as the pass element. The internal controller is a wide band transconductance amplifier capable to source current at least 1mA, which is sufficient to deliver 50mA or more output current. Typically, the JTMA7130/1/2 could support gate-off voltage (V_{GOFF}) ranges from -5V to -25V. A fault comparator is also included for monitoring the output voltage. The undervoltage threshold is set at 170mV above the 0.25V reference level.

Both the regulators are enabled after the REF voltage exceeds 1.0V. Each time it is enabled, the controller ramps up its internal reference for soft-start.

Operational Amplifier

The JTMA7130/1/2 has 1, 3 and 5 amplifiers respectively. The op amps are typically used to drive the TFT-LCD backplane (VCOM) or the gamma-correction divider string. They are featured with rail-to-rail input and output capability; furthermore, they are unity gain stable and have low power consumption (typical 0.7mA per amplifier). The JTMA7130/1/2 has a -3dB bandwidth of 10MHz while maintaining a 13V/μs slew rate.

Short Circuit Current Limit

The JTMA7130/1/2 will limit the short circuit current to ±150mA if the output is directly shorted to the SUP or BGND. If an output is shorted for a long time, the junction temperature will trigger the Over Temperature Protection, hence, the part will shutdown.

Driving Capacitive Loads

The JTMA7130/1/2 can drive a wide range of capacitive loads. As load capacitance increases, however, the -3dB bandwidth of the device will decrease and the peaking will increase. If less peaking is desired in these applications, a small series resistor (usually between 5& and 50&) can be placed in series with the output. However, this will obviously reduce the gain. Another method of reducing peaking is to add a “snubber” circuit at the output. A snubber is a shunt load consisting of a resistor in series with a capacitor. Values of 150& and 10nF are typical. The advantage of a snubber is that it does not draw any DC load current and reduce the gain.

Switch-Control Block

The switch-control input (CTL) is not activated until all four of the following conditions are satisfied: the input voltage exceeds V_{UVLO}, the soft-start routine of all the regulators is complete, there is no fault condition detected, and V_{DEL} exceeds its turn-on threshold. Once activated and if CTL is high, the 5& internal p-channel switch (Q1) between COM and SRC turns on and the 30& p-channel switch (Q2) between DRN and COM turns off. If CTL is low, Q1 turns off and Q2 turns on.

IN Under-Voltage Lockout (UVLO)

The Under-Voltage Lockout (UVLO) circuit compares the input voltage at IN with the UVLO threshold (2.5V rising, 2.4V falling, typ) to ensure the input voltage is high enough for reliable operation. The 100mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, startup begins. When the input voltage falls below the UVLO falling threshold, the controller turns off the converter.

Reference Voltage

The reference output is normally 1.25V and can source at least 100μA. Bypass REF with a 0.22μF ceramic capacitor is connected between REF and AGND.

Power-Up Sequence and Soft-Start

Figure 6 shows a detailed start-up sequence waveform. When the input voltage exceeds 2.5V, an internal current source starts to charge the REF bypass capacitor (C_{REF}) which affects the soft-start ramp. For the 0.22μF capacitor, the soft-start time is approximate 1ms. When the reference voltage exceeds 1.0V, the device enables the main step-up regulator, the gate-on linear-regulator and gate-

Function Description (Cont.)

Power-Up Sequence and Soft-Start (Cont.)

off linear-regulator controller simultaneously. The device employs soft-start for each regulator to minimize inrush current and voltage overshoot. The step-up regulator increases the current-limit level in 8 steps to limit the input current surge. Therefore, the start-up time mainly depends on the output capacitor and load current. The function prevents possible voltage drops of the input voltage. The maximum load current is available after soft-start timer expired. Both linear-regulators start-up by rising up the ramp voltage connected to the one of the positive inputs of the error amplifier. The ramp voltage replaces the reference voltage (1.233V typical) until reaches the reference voltage. The soft-start duration is 14ms (typical) for all three regulators.

A capacitor (C_{DEL}) from DEL to AGND determines startup delay time of the switch-control-block. After all three regulators are completed and there is no fault detected, a 5µA current source starts charging C_{DEL}. Once the capacitor voltage exceeds 1.25V (typ), the switch-control block is enabled as shown in Figure 6. Before startup and when IN is less than VUVLO, DEL is internally connected to AGND to discharge C_{DEL}. Select C_{DEL} to set the delay time by using the following equation:

$$C_{DEL} = Delay\_Time \cdot \frac{5\mu A}{1.25V}$$

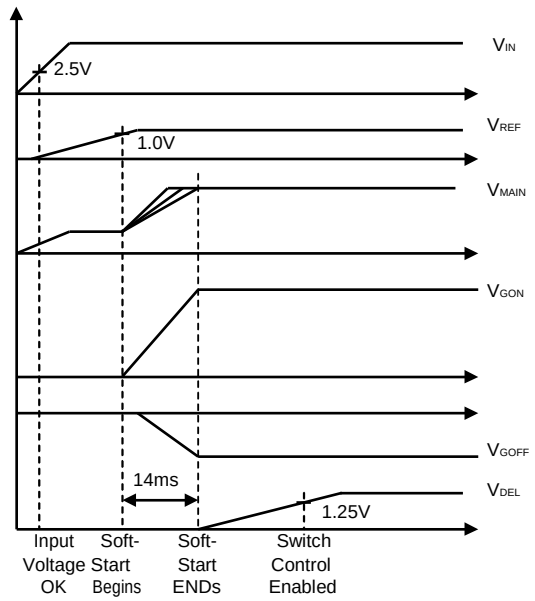


Figure 6. Start-up sequence

Fault Protection

The JTMA7130/1/2 has an advanced fault detection system that protects the IC from both adjacent pin shorts during operation and shorts on any output supplies. A high quality layout of grounding quality and decoupling is necessary to avoid falsely triggering the fault detection scheme. If the output of the main regulator or any of the linear-regulator outputs does not exceed its respective fault-detection threshold, the device activates an internal fault timer. When the fault-timer was set exceeding 120ms (typical), the device sets the fault latch to shut down all the outputs except the reference.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the JTMA7130/1/2. When the junction temperature exceeds 150°C, the thermal sensor shutdown the device.

Application Information

Step-Up Converter

Input Capacitor Selection

The input capacitor (C_{IN}) reduces the current peaks drawn from the input supply and noise injection into the IC. It is recommended that C_{IN} be larger than 10μF. The reflected ripple voltage will be smaller with larger input capacitors. For reliable operation, it is recommended to select the capacitor voltage rating at least 1.2 times higher than the maximum input voltage. The capacitors should be placed close to the IN and GND.

Output Capacitor of Boost Selection

The current-mode control scheme of the JTMA7130/1/2 allows the usage of tiny ceramic capacitors. The higher capacitor value provides the good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

$$\Delta V_{MIAN} = \Delta V_{ESR} + \Delta V_C$$

$$\Delta V_{ESR} = I_{PEAK} \cdot R_{ESR}$$

$$\Delta V_C = \frac{I_{MAIN}}{C_{OUT}} \cdot \left(\frac{V_{MAIN} - V_{IN}}{V_{MAIN} \cdot R_{ESR}} \right)$$

where I_{PEAK} is the peak inductor current.

For low ESR ceramic capacitors, the output ripple is dominated by the charging and discharging of the output capacitor. The voltage rating of the output capacitor should be greater than the maximum output voltage.

For ceramic capacitor application, the output voltage ripple is dominated by the ΔV_{COUT}. When choosing the input and output ceramic capacitors, the X5R or X7R with their good temperature and voltage characteristics are recommended.

Inductor Selection

The inductor needs a low dc resistance to decrease conduction losses and performance higher efficiency because the main material has a stronger impact on efficiency, especially on high-switching frequencies. The efficiency is moderated whilst using small chip inductor for higher inductor core losses. Therefore, it is necessary to take further consideration while choosing adequate inductor.

Mainly, the inductor value will determine the inductor ripple current: larger inductor value will result in smaller inductor ripple current and lower conduction losses of the converter. Otherwise, larger inductor value generates slower load transient response. A sensible starting point of setting ripple current is 30% to 50% of the average inductor current. The advocated inductor value can be obtained as below,

$$L \geq \left(\frac{V_{IN}}{V_{MAIN}} \right)^2 \cdot \frac{V_{MAIN} - V_{IN}}{F_{SW} \cdot I_{MAIN(MAX)}} \cdot \frac{1}{\left(\frac{\Delta I_L}{I_{L(AVG)}} \right)}$$

where

V_{IN} = input voltage

V_{MAIN} = output voltage

F_{SW} = switching frequency in MHz

I_{MAIN} = maximum output current in amp.

η = Efficiency

$\Delta I_L / I_{L(AVG)}$ = inductor ripple current/average current (0.3 to 0.5 typical)

To avoid saturation of the inductor, the inductor should be rated at least for the maximum input current of the converter plus the inductor ripple current. The maximum input current is calculated as below:

$$I_{IN(MAX)} = \frac{I_{MAIN(MAX)} \times V_{MAIN}}{V_{IN} \times \eta}$$

The peak inductor current is calculated as following equation:

$$I_{PEAK} = I_{IN(MAX)} + \frac{1}{2} \cdot \frac{V_{IN} \times (V_{MAIN} - V_{IN})}{f \times L \times V_{MAIN}}$$

Diode Selection

To achieve high efficiency, an Schottky diode must be used. The current rating of the diode must meet the peak current rating of the converter. The average of diode current is equal to load current.

Output Voltage Setting

The output voltage is set by a resistive divider. The external resistive divider is connected to the output, allowing remote voltage sensing as shown in “Typical Application Circuits”. A suggestion of the maximum value of R1 is 200k& and R2 is 20k& to keep the minimum current that provides enough noise rejection ability through the re-

Application Information (Cont.)

Output Voltage Setting (Cont.)

sistor divider. The output voltage can be calculated as below:

$$V_{MAIN} = V_{REF} \cdot \left(1 + \frac{R1}{R2}\right) = 1.233 \cdot \left(1 + \frac{R1}{R2}\right)$$

Charge Pump

To generate an output voltage higher than V_{MAIN}, single or multiple stages of charge pumps are needed. The number of stage is determined by the input and output voltage.
For positive charge pump stages:

$$N_{POSITIVE} \geq \frac{V_{GON} + V_{CE} - V_{INPUT}}{V_{INPUT} - 2 \cdot V_F}$$

Where V_{CE} is the dropout voltage of the pass transistor of the linear regulator. It ranges from 0.3V to 1V depending on the transistor selected. V_F is the forward voltage of rectifier diode. The V_{INPUT} is the input voltage of charge pump.
The number of the negative charge pump stages is given by:

$$N_{NEGATIVE} \geq \frac{-V_{GOFF} + V_{CE}}{V_{INPUT} - 2 \cdot V_F}$$

Charge Pump Capacitor Selection

Ceramic capacitor with low ESR is recommended. With ceramic capacitors, the output ripple voltage is dominated by the capacitance value. The capacitance value can be chosen by the following equation:

$$C_{CP} \geq \frac{I_{OUT\_CP}}{2 \cdot F_{SW} \cdot V_{RIPPLE\_CP}}$$

where

C_{CP} = charge pump output capacitor

I_{OUT_CP} = charge pump output current

V_{RIPPLE_CP} = charge pump ripple voltage

Charge-Pump Rectifier Diode Selection

Select the silicon diodes with a current rating equal to or greater than two times the average charge pump input current.

Linear-Regulator Controller

Output Voltage Setting

Refer to “Typical Application Circuit”, the V_{GON} and V_{GOFF} could be determined as below:

$$V_{GON} = V_{FBP} \cdot \left(1 + \frac{R3}{R4}\right) = 1.25 \cdot \left(1 + \frac{R3}{R4}\right)$$

$$V_{GOFF} = \frac{V_{FBN} \cdot (R5 + R6) - V_{REF} \cdot R6}{R5}$$

Layout Consideration

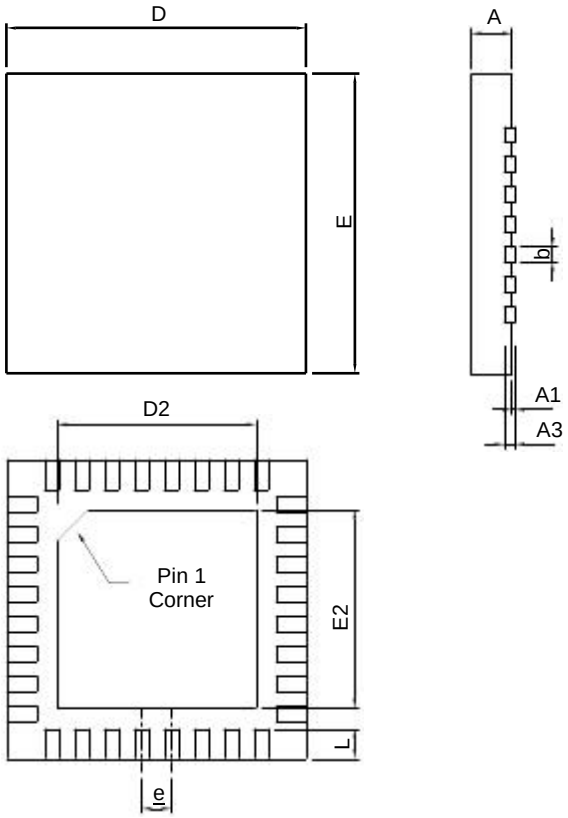
For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. There are some general guidelines for layout:

1. Place the external power components (the input capacitors, output capacitors, boost inductor and output diodes, etc.) in close proximity to the device. Traces to these components should be kept as short and wide as possible to minimize parasitic inductance and resistance.
2. Place the REF and IN bypass capacitors close to the pins. The ground connection of the IN bypass capacitor should be connected directly to the AGND pin with a wide trace.
3. Create a power ground (PGND) and a signal ground island and connect at only one point. The power ground consisting of the input and output capacitor grounds, PGND pin, and any charge-pump components. Connect all of these together with short, wide traces or a small ground plane. Maximizing the width of the power ground traces improves efficiency and reduces output voltage ripple and noise spikes. The analog ground plane (AGND) consisting of the AGND pin, all the feedback-divider ground connections, the operational-amplifier divider ground connections, the COMP and DEL capacitor ground connections, and the device's exposed backside pad. Connect the AGND and PGND islands by connecting the PGND pin directly to the exposed backside pad. Make no other connections between these separate ground planes.
4. The feedback network should sense the output voltage directly from the point of load, and be as far away from LX node as possible.
5. The exposed die plate, underneath the package, should be soldered to an equivalent area of metal on the PCB. This contact area should have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers, if available, to maximize thermal dissipation away from the IC.
6. To minimize the thermal resistance of the package when soldered to a multi-layer PCB, the amount of copper track and ground plane area connected to the exposed die plate should be maximized and spread out as far as possible from the IC. The bottom and top PCB areas especially should be maximized to allow thermal dissipation to the surrounding air.
7. Minimize feedback input track lengths to avoid switching noise pick-up.

Rev. A.1 - Mar., 2008

Package Information

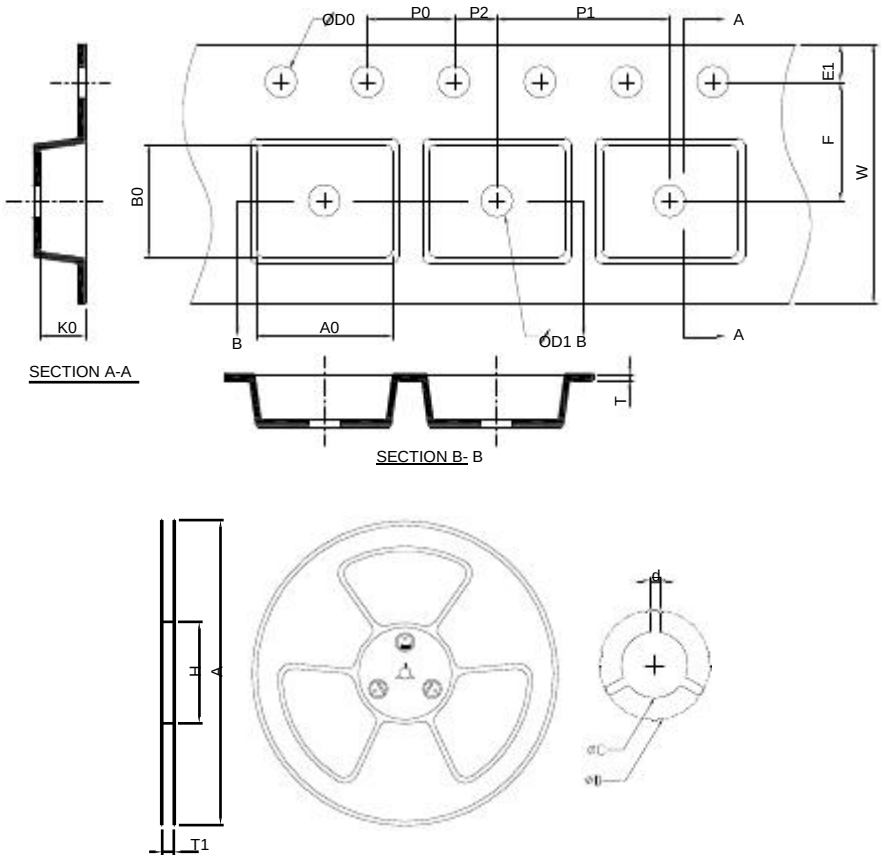
TQFN5x5-32



SYMBOL	TQFN5x5-32			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	5.00 BSC		0.197 BSC	
D2	3.50	3.80	0.138	0.150
E	5.00 BSC		0.197 BSC	
E2	3.50	3.80	0.138	0.150
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018

Note : Follow JEDEC MO-220 WHHD-4.

Carrier Tape & Reel Dimensions



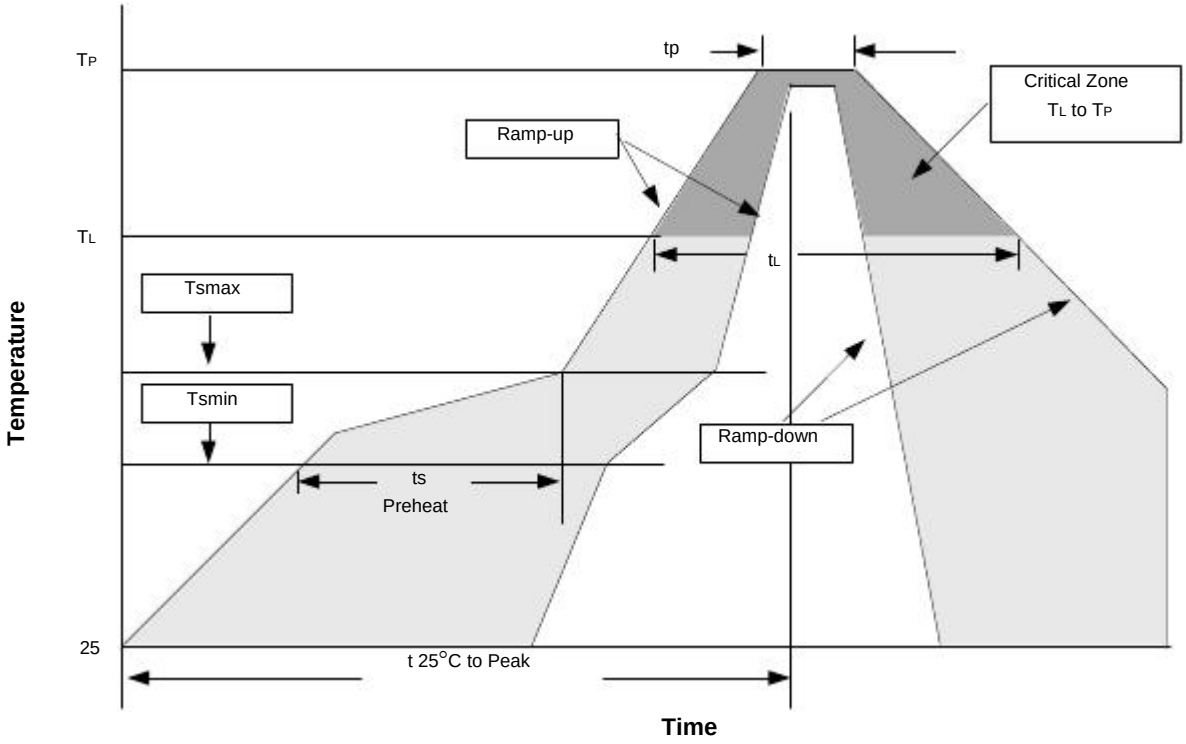
Application	A	H	T1	C	d	D	W	E1	F
TQFN5x5-32	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	12.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.30±0.20	5.30±0.20	1.30±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
TQFN5x5-32	Tape & Reel	2500

Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B, A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classification Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Note: All temperatures refer to topside of the package. Measured on the body surface.

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ε350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
ε2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
ε2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

Customer Service