

JTMA7095/A

6-Channel DC/DC Converter Control IC

Features

- Supports for Synchronous Rectification (CH1, CH2, and CH5)
- Supports for Down or Up-Down Zeta Conversions (CH1 and JTMA7095 CH2)
- Supports for Up, Flyback, or Up-Down SEPIC Conversions (JTMA7095A CH2, CH3, JTMA7095 CH4, CH5, and CH6)
- Supports for Inverting Conversion (JTMA7095A CH4)
- Low Start-up Voltage : 1.4V (CH6)
- Power Supply Voltage Range
 - CH1 to CH5 : 3.0V to 6.5V
 - CH6 : 2.4V to 6.5V
- 1% Reference Voltage Accuracy
- Wide Operating Frequency 100kHz to 1MHz
- Soft-Start Function (CH1 to 6)
- Power Good (PGOOD) Indicator for CH1
- Low Shutdown Current
- Output Short-Circuit Detections
- Lead Free and Green Devices Available (RoHS Compliant)

General Description

The JTMA7095/A is a 6-channel, frequency-settable, voltage-mode, DC/DC control IC providing a complete power supply solution for high-performance portable digital cameras. The JTMA7095/A uses pulse-width-modulation (PWM) and synchronous rectification for high efficiency step-up, step-down, up-down, and inverting converters with free input and output settings in 2 or 4-cell AA, 1-cell lithium-ion (Li+), and dual-battery designs. The JTMA7095/A incorporates error amplifiers, output short-circuit detection, under-voltage lockout, soft-start, and output switch control into a chip. The AP7095/A improves performance, component count, and size compared to conventional multi-channel controllers.

The JTMA7095/A has a power-good indicator (PGOOD) that signals when CH1 output is within $\pm 10\%$ of the set voltage by monitoring IN1 pin.

The JTMA7095/A is available in compact 48-pin plastic LQFP and TQFN packages.

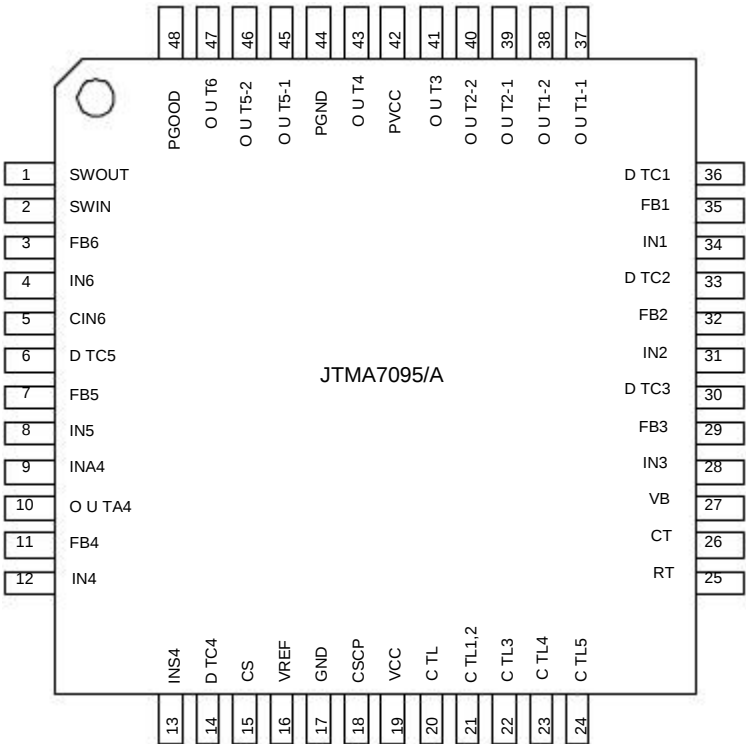
Applications

- Digital Camera
- Camcorder
- Hand-Held Instrument

JIATAIMU reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

JTMA7095/A Assembly Material Handling Code Temperature Range Package Code	Package Code QD : LQFP7x7-48 QB : TQFN7x7-48 Operating Ambient Temperature Range E : -30 to 85 °C Handling Code TB : Tape & Box TR : Tape & Reel Assembly Material L : Lead Free Device G : Halogen and Lead Free Device
JTMA7095 QD/QB : JTMA7095 XXXXX	XXXXXX - Date Code
JTMA7095A QD/QB : JTMA7095A XXXXX	XXXXXX - Date Code

Note: JIATAIMU lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. JIATAIMU lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. JIATAIMU defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).



IC	JTMA7095	JTMA7095A
CH1	Synchronous Step-down	Synchronous Step-down
CH2	Synchronous Up-down	Synchronous Step-up
CH3	Step-up	Step-up
CH4	Step-up	Inverting
CH5	Synchronous Step-up	Synchronous Step-up
CH6	Step-up	Step-up

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Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V _{CC}	VCC Supply Voltage (VCC to GND)	-0.3 ~ 7	V
V _{PVCC}	PVCC Supply Voltage (PVCC to GND)	-0.3 ~ 7	V
	IN1~6, INA4, INS4, DTC1~5 Input Voltages	-0.3 ~ V _{CC} +0.3	V
	CTL, CTL1~5, SWIN Input Voltages	-0.3 ~ 7	V
	PGOOD Pull High Voltage	-0.3 ~ 7	V
	Maximum Junction Temperature	150	°C
T _{STG}	Storage Temperature	-65 ~ 150	°C
T _{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air 48-pin Plastic LQFP	80	°C/W

Recommended Operating Conditions

Symbol	Parameter	Conditions	JTMA7095/A			Unit
			Min.	Typ.	Max.	
V _{CC}	Start-up Power Supply Voltage	CH6	1.4	-	6.5	V
V _{CC}	Operating Voltage	CH6	2.4	5.0	6.5	V
		CH1 to CH5	3.0	5.0	6.5	
I _{REF}	Reference Voltage Output Current	VREF Pin	-1	-	0	mA
I _B	VB Output Current	VB Pin	-0.5	-	0	mA
V _{IN}	Input Voltage	IN1 to IN5, INA4, INS4 Pins	0	-	V _{CC}	V
		IN6 Pin	0	-	V _{CC}	
V _{CTL}	Control Voltage	CTL Pin	0	-	6.5	V
I _O	Output Current	OUT Pin (CH1 to CH5)	-	2	15	mA
		OUT Pin (CH6)	-	2	15	
		SWOUT Pin	-	1	4	
F _{OSC}	Oscillator Frequency		100	500	1000	kHz
C _T	Timing Capacitor		47	100	560	pF
R _T	Timing Resistor		8.2	18	100	kΩ
C _S	Soft-Start Capacitor	CH1 to CH5	-	0.027	1.0	μF
C _{CIN6}		CH6	-	0.47	1.0	

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Recommended Operating Conditions (Cont.)

Symbol	Parameter	Conditions	JTMA7095/A			Unit
			Min.	Typ.	Max.	
C _{SCP}	Short Detection Capacitor		-	0.1	1.0	∞F
C _{VB}	VB Pin Capacitor		0.082	0.1	-	∞F
T _A	Operating Ambient Temperature		-30	25	85	°C

Electrical Characteristics

Refer to the typical application circuit. These specifications apply over, V_{CC} = 5V and T_A = -30 to 85°C, unless otherwise specified. Typical values refer to T_A = 25°C.

Symbol		Parameter	Test Conditions	JTMA7095/A			Unit
				Min.	Typ.	Max.	
I _{CCS}	VCC	Standby Current	CTL = 0V	-	-	10	∞A
I _{PVCC}	PVCC	Standby Current	CTL = 0V	-	-	10	
I _{CC}	VCC	Nominal Supply Current	CTL, CTL1 to CTL5 = 5V	-	1.8	5	mA
UNDER VOLTAGE LOCKOUT							
V _{TH}	CH1 to CH5	Threshold Voltage	Rising V _{CC}	2.5	2.7	2.9	V
V _H		Hysteresis Width		-	0.2	-	
V _{RST}		Reset Voltage	Falling V _{CC}	1.2	1.3	1.4	
V _{TH}	CH6	Threshold Voltage	Rising V _{CC}	1.25	1.4	1.55	
REFERENCE VOLTAGE							
V _{REF}	Reference Voltage		I _{REF} = 0mA	2.46	2.49	2.51	V
□V _{REF} /V _{REF}	Output Voltage Temperature Stability		T _A = -30°C to 85°C	-	0.5	-	%
Line	Input Stability		V _{CC} = 3.0V to 6.5V	-10	-	10	mV
Load	Load Stability		I _{REF} = 0mA to -1mA	-10	-	10	mV
I _{OS}	Short-Circuit Output Current		V _{REF} = 2V	-25	-18	-1	mA
SOFT-START							
V _{STB}	Input Standby Voltage			-	50	100	mV
I _{CS}	Soft-Start Charge Current			-1.4	-1.0	-0.6	∞A
SHORT-CIRCUIT DETECTION							
V _{TH}	Threshold Voltage			0.65	0.70	0.75	V
V _{STB}	Input Standby Voltage			-	50	100	mV
V _I	Input Latch Voltage			-	50	100	mV
I _{CSCP}	Input Source Current			-1.4	-1.0	-0.6	∞A
TRIANGULAR WAVE OSCILLATOR							
f _{OSC}	Oscillator Frequency		CT=100pF, RT=18k&,VB=2V	450	500	550	kHz
□f/f _{dv}	Frequency Stability for Voltage		VCC = 3V to 6.5V	-	1	10	%
□f/f _{dt}	Frequency Stability for Temperature		T _A = -30°C to 85°C	-	1	-	%
ERROR AMPLIFIER (CH1 to CH5)							
V _{TH}	Threshold Voltage		FB = 1.45V	1.23	1.25	1.27	V
□V _T /V _T	V _T Temperature Stability		T _A = -30°C to 85°C	-	0.5	-	%

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Electrical Characteristics (Cont.)

Refer to the typical application circuit. These specifications apply over, $V_{CC}=5V$ and $T_A=-30$ to $85^{\circ}C$, unless otherwise specified. Typical values refer to $T_A=25^{\circ}C$.

Symbol	Parameter	Test Conditions	JTMA7095/A			Unit
			Min.	Typ.	Max.	
ERROR AMPLIFIER (CH1 to CH5) (Cont.)						
I _B	Input Bias Current	IN = 0V (CH1 to CH5)	-50	-	-	nA
A _v	Voltage Gain	DC	60	100	-	dB
BW	Frequency Bandwidth	A _v = 0dB	-	1.0	-	MHz
V _{OH}	Maximum Output Voltage		4.9	4.99	-	V
V _{OL}	Minimum Output Voltage		-	3	50	mV
I _{SOURCE}	Output Source Current	FB = 1.45V	-	-25	-10	mA
I _{SINK}	Output Sink Current	FB = 1.45V	5	16	-	mA
ERROR AMPLIFIER (CH6)						
V _{TH}	Threshold Voltage	FB = 0.55V	1.24	1.26	1.28	V
$\frac{\Delta V_{TH}}{V_{TH}}$	V _{TH} Temperature Stability	T _A = -30°C to 85°C	-	0.5	-	%
I _B	Input Bias Current	IN6 = 0V	-50	-	-	nA
A _v	Voltage Gain	DC	60	75	-	dB
BW	Frequency Bandwidth	A _v = 0dB	-	1.0	-	MHz
V _{OH}	Maximum Output Voltage		4.9	4.99	-	V
V _{OL}	Minimum Output Voltage		-	3	50	mV
I _{SOURCE}	Output Source Current	FB = 0.55V	-	-50	-10	mA
I _{SINK}	Output Sink Current	FB = 0.55V	60	120	-	∞A
INVERTED AMPLIFIER (CH4)						
V _{IO}	Input Offset Voltage	OUT = 1.25V	-10	0	10	mV
I _B	Input Bias Current	IN = 0V	-50	-	-	nA
A _v	Voltage Gain	DC	60	100	-	dB
BW	Frequency Bandwidth	A _v = 0dB	-	1.0	-	MHz
V _{OH}	Maximum Output Voltage		4.9	4.99	-	V
V _{OL}	Minimum Output Voltage		-	3	50	mV
I _{SOURCE}	Output Source Current	OUT = 1.25V	-	-26	-1.0	mA
I _{SINK}	Output Sink Current	OUT = 1.25V	5	16	-	mA
SHORT DETECT COMPARATOR (CH1 to CH5)						
V _{TH}	Threshold Voltage	CH1 to CH5	0.97	1.00	1.03	V
I _B	Input Bias Current	IN = 0V (CH1 to CH3, CH5)	-50	-	-	nA
		INS4 = 0V (CH4)	-50	-	-	
SHORT DETECT COMPARATOR (CH6)						
V _{TH}	Threshold Voltage		0.8	0.9	1.0	V
PWM COMPARATOR (CH1 to CH5)						
V _{T0}	Threshold Voltage	Duty = 0%	1.0	1.1	-	V
V _{T100}		Duty = 100%	-	1.8	1.9	
I _{DTC}	Input Current	DTC = 0.4V (CH1 to CH5)	-50	-	-	nA

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Electrical Characteristics (Cont.)

Refer to the typical application circuit. These specifications apply over, $V_{CC}=5V$ and $T_A = -30$ to $85^{\circ}C$, unless otherwise specified. Typical values refer to $T_A = 25^{\circ}C$.

Symbol	Parameter	Test Conditions	JTMA7095/A			Unit
			Min.	Typ.	Max.	
PWM COMPARATOR (CH6)						
V _{T0}	Threshold Voltage	Duty = 0%	0.2	0.3	-	V
V _{Tmax}		Duty = Max.	-	0.74	0.84	
D _{tr}	Maximum Duty Cycle	CT = 100pF, RT = 18kΩ	70	80	90	%
PWM CONTROLLER DRIVER FOR P-MOS (CH1, CH2, CH5)						
I _{SOURCE}	Output Source Current	Duty δ 5%, OUT = 0V	-	-130	-80	mA
I _{SINK}	Output Sink Current	Duty δ 5%, OUT = 5V	100	160	-	
R _{OH}	Output ON Resistance	OUT = -15mA	-	18	30	&
R _{OL}		OUT = 15mA	-	10	20	
PWM CONTROLLER DRIVER FOR N-MOS (CH1, CH2, CH5, CH6)						
I _{SOURCE}	Output Source Current	Duty δ 5%, OUT = 0V	-	-130	-80	mA
I _{SINK}	Output Sink Current	Duty δ 5%, OUT = 5V	100	160	-	
R _{OH}	Output ON Resistance	OUT = -15mA	-	18	30	&
R _{OL}		OUT = 15mA	-	10	20	
PWM CONTROLLER DRIVER FOR P-MOS (CH3, CH4)						
I _{SOURCE}	Output Source Current	Duty δ 5%, OUT = 0V	-	-290	-180	mA
I _{SINK}	Output Sink Current	Duty δ 5%, OUT = 5V	300	470	-	
R _{OH}	Output ON Resistance	OUT = -15mA	-	7	15	&
R _{OL}		OUT = 15mA	-	4	10	
OUTPUT SWITCH CONTROL (SW)						
V _{IH}	SW Input Voltage	SWOUT = "L" level	1.2	-	6.5	V
V _{IL}		SWOUT = "H" level	0	-	0.5	
I _{SWIN}	Input Current	SWIN = 5V	-	2.5	20	∞A
I _{SOURCE}	Output Source Current	SWOUT = 0V	-	-7	-	mA
I _{SINK}	Output Sink Current	SWOUT = 5V	-	19	-	mA
R _{OH}	Output ON Resistance	OUT = -4mA	-	325	400	&
R _{OL}		OUT = 4mA	-	85	150	
POWER GOOD						
V _{TH}	IN1 Upper Threshold Voltage	Rising IN1	-	110	-	%
V _{TH}	IN1 Lower Threshold Voltage	Rising IN1	-	94	-	%
	Upper/Lower Hysteresis		-	2	-	%
V _{PGOOD}	PGOOD Output Voltage	I _{PGOOD} = 4mA	-	0.17	0.8	V
CONTROL BLOCK (CTL, CT1 to CT5)						
V _{IH}	CTL Input Voltage	Active Mode	1.5	-	6.5	V
V _{IL}		Standby Mode	0	-	0.5	
I _{CTL}	Input Current	CTL = 5V	-	2.6	20	∞A

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Pin Description

PIN		I/O	FUNCTION
NO.	NAME		
1	SWOUT	O	Output Switch Control Circuit Output Pin.
2	SWIN	I	Output Switch Control Circuit Input Pin.
3	FB6	O	CH6 Error Amplifier Output Pin.
4	IN6	I	CH6 Inverted Input Pin of Error Amplifier.
5	CIN6	I	CH6 Soft-Start Capacitor Connection Pin. Leave this pin "Open" to disable the soft-start function.
6	DTC5	I	CH5 Dead Time Control Pin. Connect this pin to VREF directly when the dead-time control is not used.
7	FB5	O	CH5 Error Amplifier Output Pin.
8	IN5	I	CH5 Inverted Input Pin of Error Amplifier.
9	INA4	I	CH4 Inverting Amplifier Input Pin.
10	OUTA4	O	CH4 Inverting Amplifier Output Pin. Connect this pin to INA4 when the inverting amplifier is not used.
11	FB4	O	CH4 Error Amplifier Output Pin.
12	IN4	I	CH4 Inverted Input Pin of Error Amplifier.
13	INS4	I	CH4 Inverted Input Pin of Short Detection Comparator.
14	DTC4	I	CH4 Dead Time Control Pin. Connect this pin to VREF directly when the dead-time control is not used.
15	CS	-	CH1 to CH5 Soft-Start Capacitor Connection Pin. Leave this pin "Open" to disable the soft-start function.
16	VREF	O	Reference Voltage Output Pin.
17	GND	P	Reference Voltage and Control Circuit Ground Pin.
18	CSCP	-	Short-Circuit Detection Capacitor Connection Pin. Connect this pin to GND with the shortest distance to disable the timer-latch short-circuit protection circuit.
19	VCC	P	Reference Voltage and Control Circuit Power Supply Pin.
20	CTL	I	Power Supply and CH6 Control Pin. "H" Level: Operation Mode. "L" Level: Standby Mode
21	CTL1,2	I	CH1 and CH2 Control Pin. "H" Level: Operation Mode. "L" Level: OFF Mode
22	CTL3	I	CH3 Control Pin. "H" Level: Operation Mode. "L" Level: OFF Mode
23	CTL4	I	CH4 Control Pin. "H" Level: Operation Mode. "L" Level: OFF Mode
24	CTL5	I	CH5 Control Pin. "H" Level: Operation Mode. "L" Level: OFF Mode

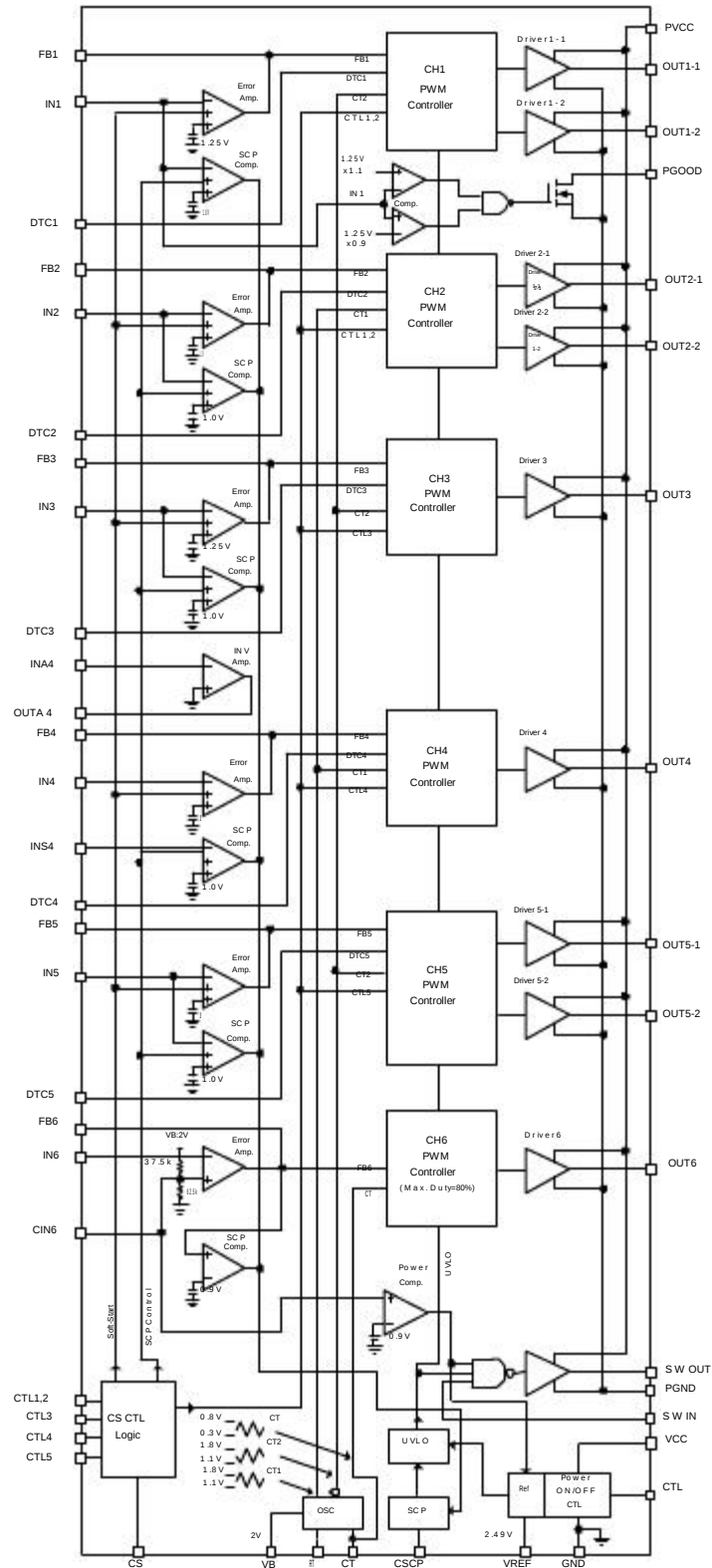
JTMA7095/A

Pin Description (Cont.)

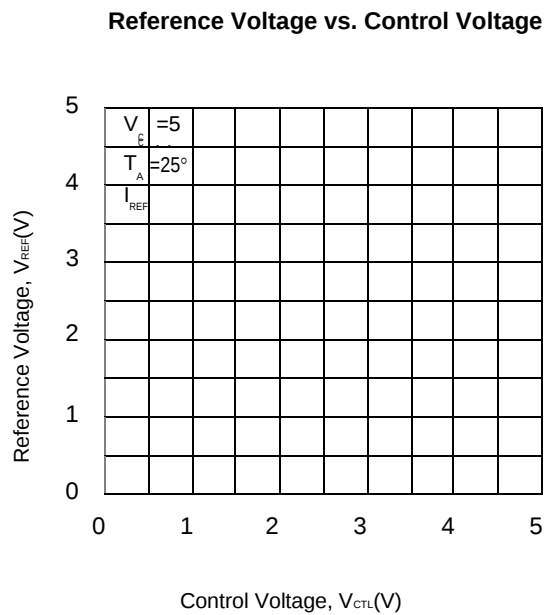
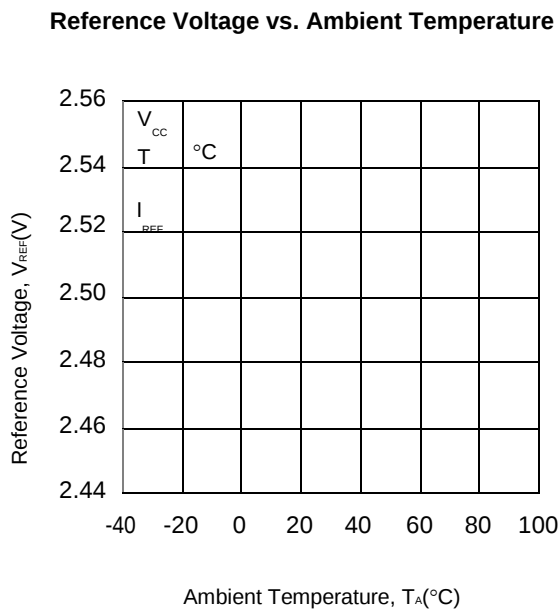
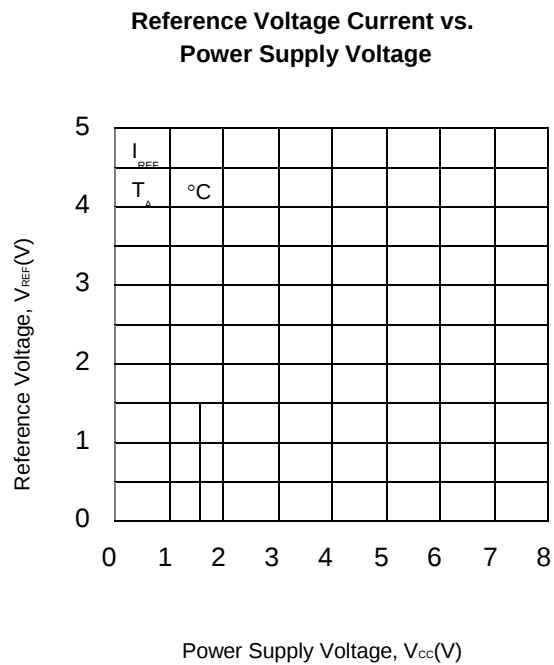
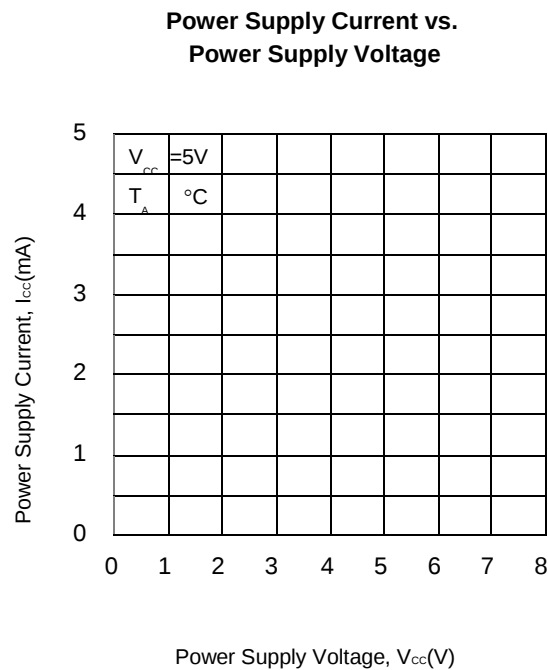
PIN		I/O	FUNCTION
NO.	NAME		
25	RT	-	Oscillator Frequency Setting Resistor Connection Pin.
26	CT	-	Oscillator Frequency Setting Capacitor Connection Pin.
27	VB	O	Triangular Wave Oscillator Regulator Output Pin.
28	IN3	I	CH3 Inverted Input Pin of Error Amplifier.
29	FB3	O	CH3 Error Amplifier Output Pin.
30	DTC3	I	CH3 Dead Time Control Pin. Connect this pin to VREF directly when the dead-time control is not used.
31	IN2	I	CH2 Inverted Input Pin of Error Amplifier.
32	FB2	O	CH2 Error Amplifier Output Pin.
33	DTC2	I	CH2 Dead Time Control Pin. Connect this pin to VREF directly when the dead-time control is not used.
34	IN1	I	CH1 Inverted Input Pin of Error Amplifier.
35	FB1	O	CH1 Error Amplifier Output Pin.
36	DTC1	I	CH1 Dead Time Control Pin. Connect this pin to VREF directly when the dead-time control is not used.
37	OUT1-1	O	CH1 Main-side MOSFET Drive Pin. Connect OUT1-1 to the main MOSFET.
38	OUT1-2	O	CH1 MOSFET Drive Pin for Synchronous Rectifier.
39	OUT2-1	O	CH2 Main-side MOSFET Drive Pin. JTMA7095: Drive a p-channel MOSFET for a step-down converter. JTMA7095A: Drive an n-channel MOSFET for a step-up converter.
40	OUT2-2	O	CH2 MOSFET Drive Pin for Synchronous Rectifier
41	OUT3	O	CH3 MOSFET Drive Pin.
42	PVCC	P	Drive Circuit Power Supply Pin.
43	OUT4	O	CH4 MOSFET Drive Pin. JTMA7095: Drive an n-channel MOSFET for a step-up converter. JTMA7095A: Drive a p-channel MOSFET for a inverting step-up/down converter.
44	PGND	P	Drive Circuit Ground Pin.
45	OUT5-1	O	CH5 Main-side MOSFET Drive Pin. Connect OUT5-1 to the main MOSFET.
46	OUT5-2	O	CH5 MOSFET Drive Pin for Synchronous Rectifier.
47	OUT6	O	CH6 MOSFET Drive Pin.
48	PGOOD	O	Indicator Output Pin. This pin is an open-drain output used to indicate status of the CH1 output voltage.

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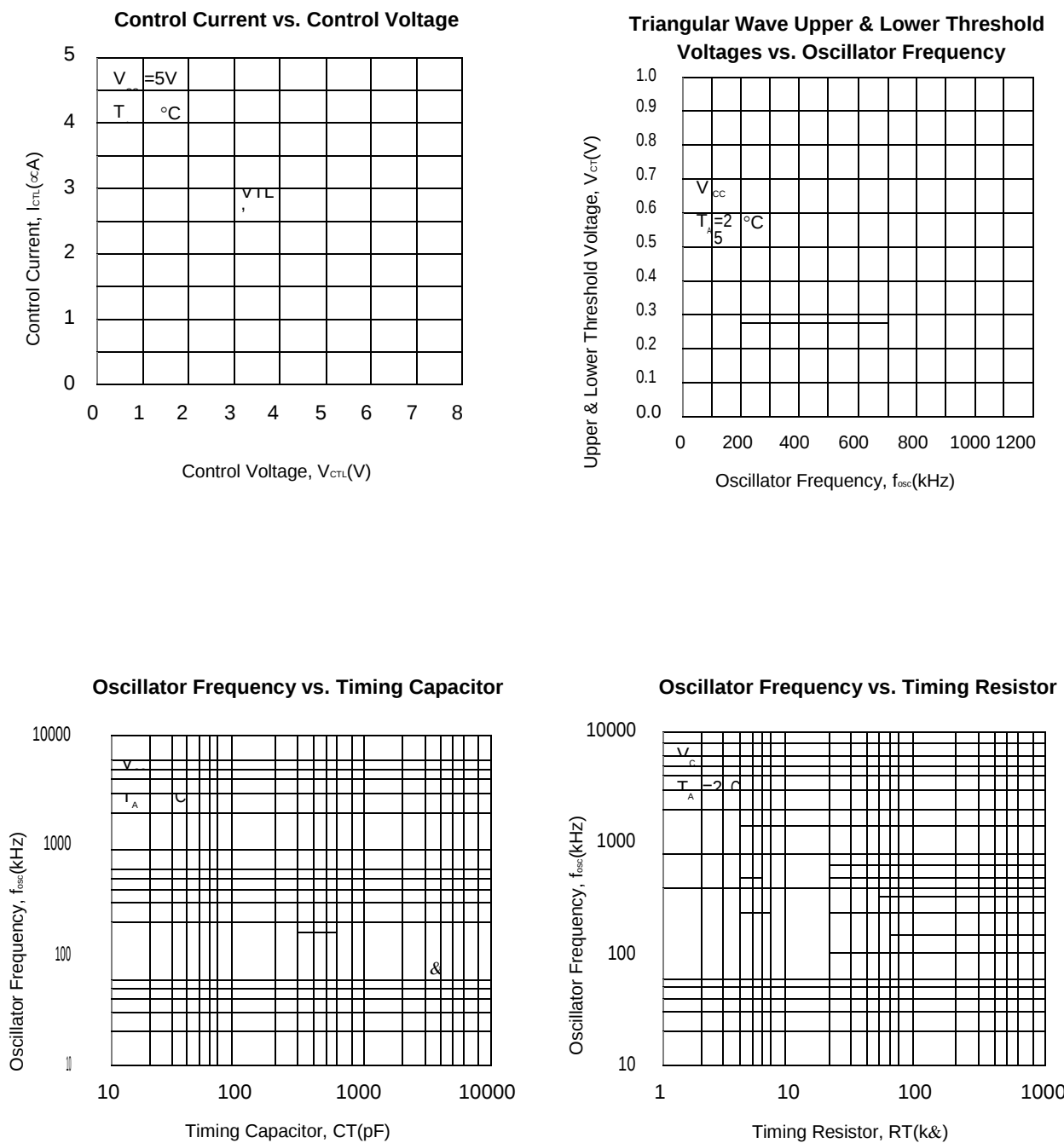
Block Diagram



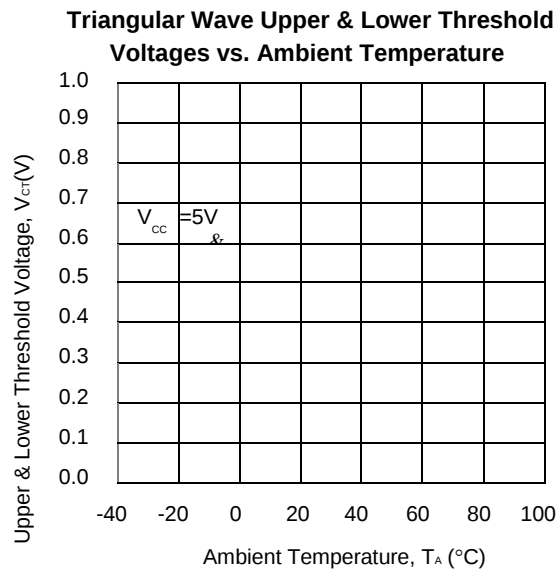
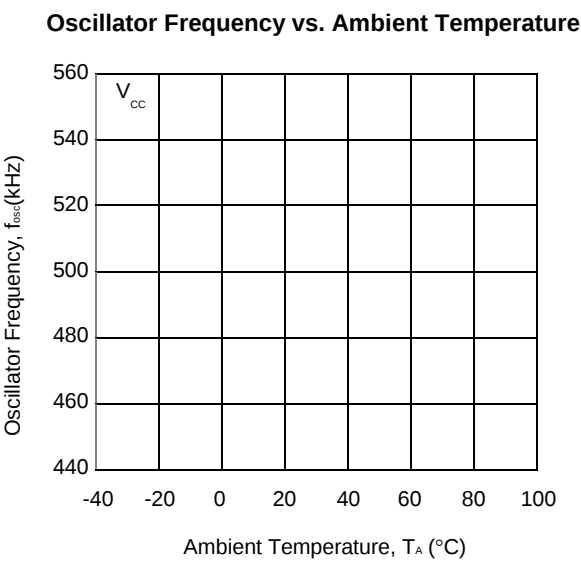
Typical Operating Characteristics



Typical Operating Characteristics (Cont.)



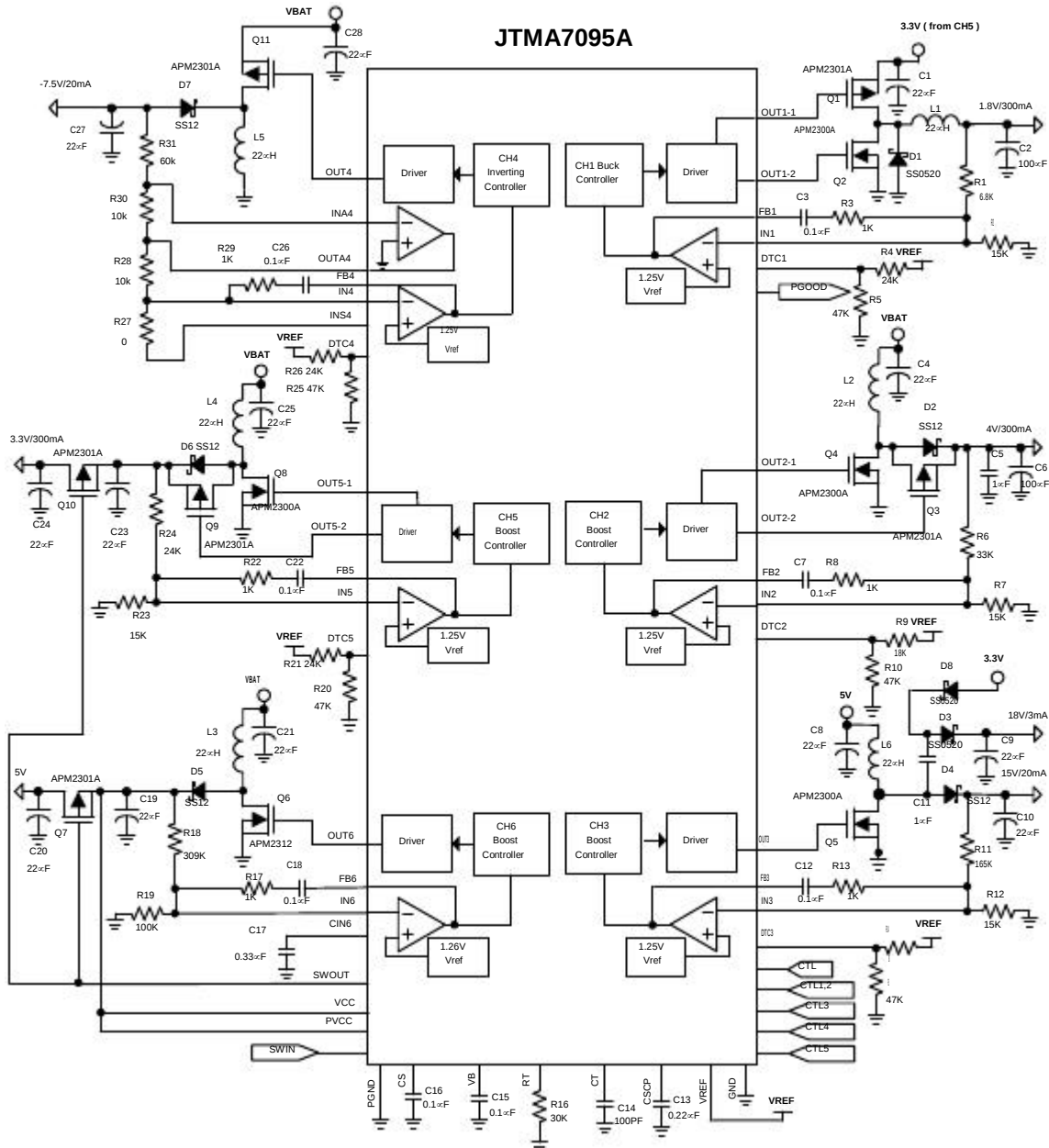
Typical Operating Characteristics (Cont.)



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Typical Application Circuit(Cont.)

2.VBAT=1.4V~3V (2-Cell Battery) for 1 Buck , 1 Inverting and 4 Boost Converter s (Using JTMA7095A)



JTMA7095/A

Function Description

General

The JTMA7095/A provides voltage-mode feedback controls for six DC/DC PWM converters(CH1 to CH6). Each channel operates with an error amplifier, PWM comparator, short-circuit comparator, ON/OFF control, and output driver. An internal temperature-compensated voltage provides reference voltages for each channel. An triangular-wave oscillator(CT) with a timing resistor and capacitor generates triangular waves to each channel. A inverting amplifier(CH4) cooperates with the error amplifier for an inverting converter (with negative output voltage) .

Reference Voltage

The JTMA7095 outputs a temperature- compensated reference voltage(2.49V) at VREF pin. It is regulated from the voltage at VCC pin and can source current of max. 1mA to external loads. It also supplies bias for the IC's internal circuitry.

Triangular-wave Oscillator

The triangular-wave oscillator is designed to generates a triangular oscillation signal (CT) with amplitude of 0.3V~0.8V at CT pin, providing signal to CH6. The oscillator frequency is settable from 100kHz to 1MHz and set by a timing resistor and a timing capacitor connected respectively from RT and CT pins to ground. Additional two triangular oscillation signals (CT1 and CT2) are also internally generated with amplitude of 1.1V~1.8V. The CT1 is in phase with the CT to the PWM comparators of CH2 and CH4; the CT2 is out of phase with the CT to the PWM comparators of CH1, CH3, and CH5.

Error Amplifier

The error amplifier is designed with unit-gain-bandwidth of 1MHz and to satisfy wide application requirements. It works with external resistor-capacitor network for each converter's feedback compensation. The loop gain can be set by connecting a feedback resistor and capacitor from the output pin(FB) to inverted input pin of the error amplifier for stable operations.

Inverting Amplifier (Inv Amp)

The inverting amplifier detects the inverting DC/DC converter output voltage (as a negative voltage) and outputs a control signal to the error amp.

Channel Control Function

The channel control function turns on/off one or more channels depending on the states ("H" or "L" level) at CTL, CTL1,2 to CTL5 pins. The on/off control logic is shown as the following table:

Channel on/off Setting Table

Voltage Level at CTL Pin					Channel ON/OFF State				
CTL	CTL1,2	CTL3	CTL4	CTL5	Power /CH6	CH1 /CH2	CH3	CH4	CH6
L	x	x	x	x	OFF(Standby State)				
H	L	L	L	L	ON	OFF	OFF	OFF	OFF
			H	H				ON	ON
			L	L				OFF	OFF
		H	L	L			ON	OFF	ON
			H	H				ON	OFF
			L	L				ON	ON
	H	L	L	L		OFF	OFF	OFF	OFF
			H	H				ON	ON
			L	L				OFF	ON
		H	L	L			ON	OFF	ON
			H	H				ON	OFF
			L	L				ON	ON

MOSFET Drive Circuits

JTMA7095/A uses push-pull configuration at output of each MOSFET driver for providing large drive current to MOSFET gate. The following table shows the MOSFETs connected to the drivers:

IC	JTMA7095	JTMA7095A
CH1	OUT1-1 : PMOS OUT1-2 : NMOS	OUT1-1 : PMOS OUT1-2 : NMOS
CH2	OUT2-1 : PMOS OUT2-2 : NMOS	OUT2-1 : NMOS OUT2-2 : PMOS
CH3	OUT3 : NMOS	OUT3 : NMOS
CH4	OUT4 : NMOS	OUT4 : PMOS
CH5	OUT5-1 : NMOS OUT5-2 : PMOS	OUT5-1 : NMOS OUT5-2 : PMOS
CH6	OUT6 : NMOS	OUT6 : NMOS

Timer-Latch Short-Circuit Protection Circuit

The short-circuit protection comparator in each channel (CH1 to CH5) monitors converter's output voltage via input pin of error amplifier. In CH6, the short-circuit comparator detects the voltage at output of error amplifier. As any detected voltages of CH1 to CH5 falls below 1.0V or the detected voltage of CH6 is larger than 0.9V, the timer circuits is actuated to start charging the external capacitor CSCP connected from CSCP pin to ground. When the rising voltage of CSCP reaches 0.7V, the IC turns off all

Function Description (Cont.)

Timer-Latch Short-Circuit Protection Circuit (Cont.)

external MOSFETs and pulls up the voltage at SWOUT pin. Then the IC is latched. Applying a signal from “L” to “H” to CTL pin enables operation again. The short-circuit detection function remains working during soft-start operation on CH1 to CH5.

Under-Voltage Lockout (UVLO) Circuit

The under-voltage lockout circuit monitors the supply voltage at VCC pin to prevent wrong logic control. The IC starts operation after the supply voltage rises above its rising threshold. As the supply voltage falls below its falling threshold, the IC turns off the external MOSFETs and pulls up the voltage at SWOUT pin.

Soft-Start Operation

The soft-start function controls the output voltage rate of rise to limit the current surge at start-up. For CH1 to CH5, the soft-start interval is programmed by the soft-start capacitor, CS connected from CS pin to ground and charged by an internal $1\mu\text{A}$ current source. For CH6, a sourcing current from the internal resistor-divider charges the capacitor, CCIN6 connected from CIN6 pin to ground, providing soft-start control.

Figure 1 and 2 show the soft-start processes. In figure 1, when all control pins (CTL, CTL1,2 to CTL 5) are driven high (“H” level) at the same time, the voltage at CIN6 pin starts to rise up by charging the capacitor CCIN6, starting a soft-start operation on CH6. After the rising voltage at CIN6 reaches 0.9V, the reference voltage starts to regulate and the internal source current starts to charge the CS, starting a soft-start operation on CH1 to CH5. During soft-start interval, the error amplifiers compares the CH1 to CH5 output voltage to the voltage at the CS pin. When any control pins (CH1,2 to CH5) go “H” from “L” during the soft-start interval (CH1 to CH5), the output rises rapidly to follow the rising voltage at CS pin.

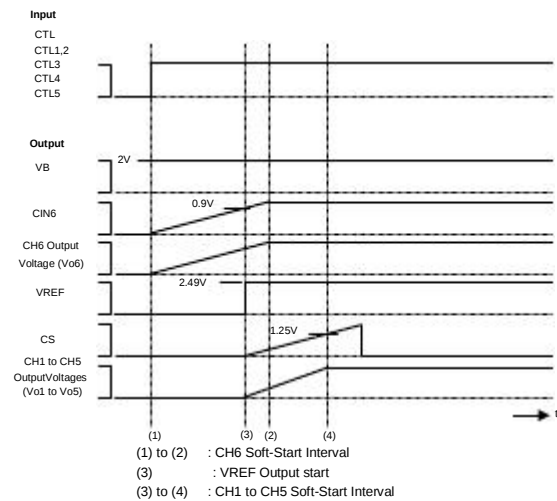


Figure 1 Soft-Start Waveforms

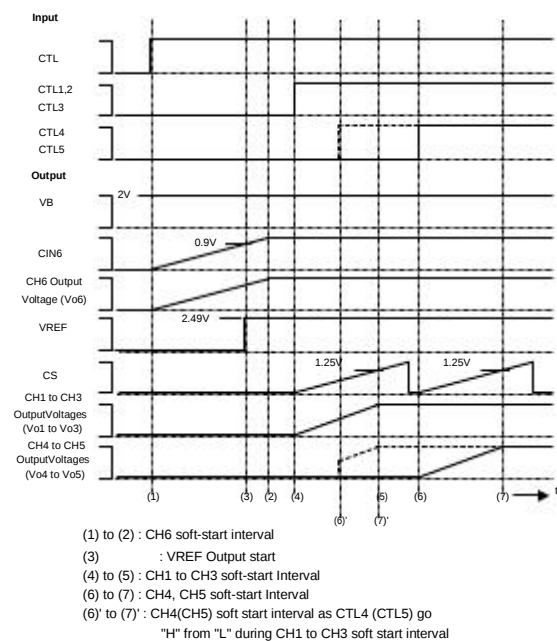


Figure 2 Soft-Start Waveforms

Output Switch Control Circuit

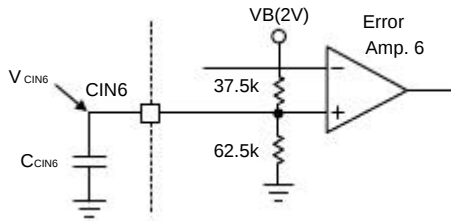
The output switch control circuit outputs a signal to control external p-channel MOSFETs for preventing reactive current flow to external step-up circuits on CH5 and CH6. When a “H” level signal is applied to SWIN pin after releasing the UVLO and the voltage at CIN6 pin rises above 0.9V(typical), the IC pulls low the voltage at SWOUT pin, turning on the external p-channel MOSFETs to generate output voltages.

Application Information

Soft-Start Interval Settings

The CH6 soft-start time depends on the capacitor CCIN6 and is determined as the following equation:

$$t_s (S) = - \frac{C_{CIN6} (F) \oplus 37.5 (k\&) \oplus 62.5 (k\&)}{100 (k\&)} \oplus \ln \left(\left| 1 + \frac{V_{CIN6} (V)}{1.26 (V)} \right| \right)$$



The soft-start time until CH6 output voltage reaches 95% of the set voltage is determined as the following equation:

$$t_s (S) \approx 0.07 \oplus C_{CIN6} (\&F)$$

On CH1 to CH5, the soft-start time depending on the capacitor CS determined as the following equation :

$$t_s (S) \approx 1.25 \oplus C_s (\&F)$$

Triangular Oscillator Frequency Setting

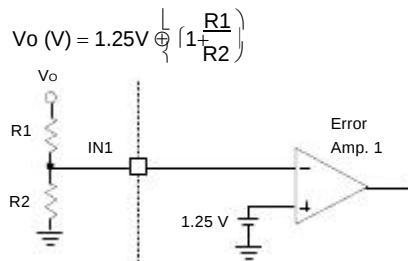
The triangular oscillator frequency set by the timing capacitor (CT) connected to the CT pin and the timing resistor (RT) connected to the RT pin determined as the following equation:

$$f_{osc} (kHz) \approx \frac{900000}{RT (k\&) \oplus CT (pF)}$$

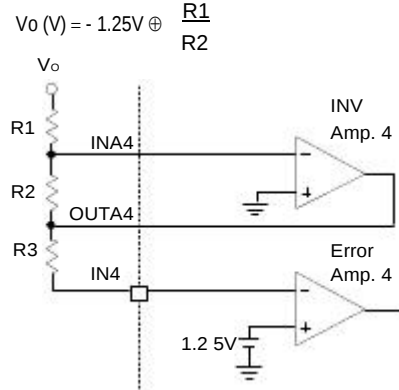
Output Voltage Settings

The output voltage is set by the external resistor-divider connected with converter output, error amplifier input, and ground.

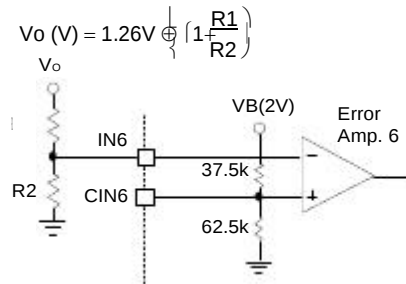
(1) CH1 to CH3, CH5



(2) CH4



(3) CH6



Time Constant Setting for Timer-Latch Short-Circuit Protection Circuit

The time constant for timer-latch short-circuit protection is set by the capacitor CSCP and determined as the following equation :

$$t_{PE} (S) \approx 0.70 \oplus C_{SCP} (\&F)$$

Dead-Time Setting

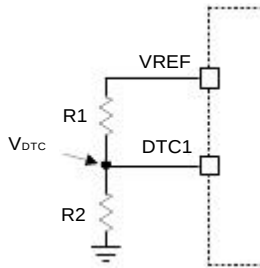
The dead-time control pin (DTC) is designed to set the maximum ON duty of the main-side MOSFET. When the device is set for step-up inverted output based on the step-up or step-up/down Zeta method or flyback method, the FB pin voltage may reach and exceed the triangular wave voltage due to load fluctuation. If this is the case, the output MOSFET is fixed to a ON duty of 100 %. To prevent this, set the maximum duty of the output MOSFET. Connecting a resistor- divider between VREF, DTC and GND pins provides a voltage VDTC to DTC pin. When the the voltage at the DTC pin is higher than the triangular wave voltage (CT1/2), the output transistor is turned on. The maximum duty is calculated as the following equation:

Application Information (Cont.)

Dead-Time Setting (Cont.)

$$\text{ON Duty}_{(\text{max})} = \frac{V_{\text{DTC}} - 1.1 \text{ V}}{0.7 \text{ V}} \oplus 100 (\%)$$

$$V_{\text{DTC}} (\text{V}) = \frac{R2}{R1 + R2} \oplus V_{\text{REF}}$$

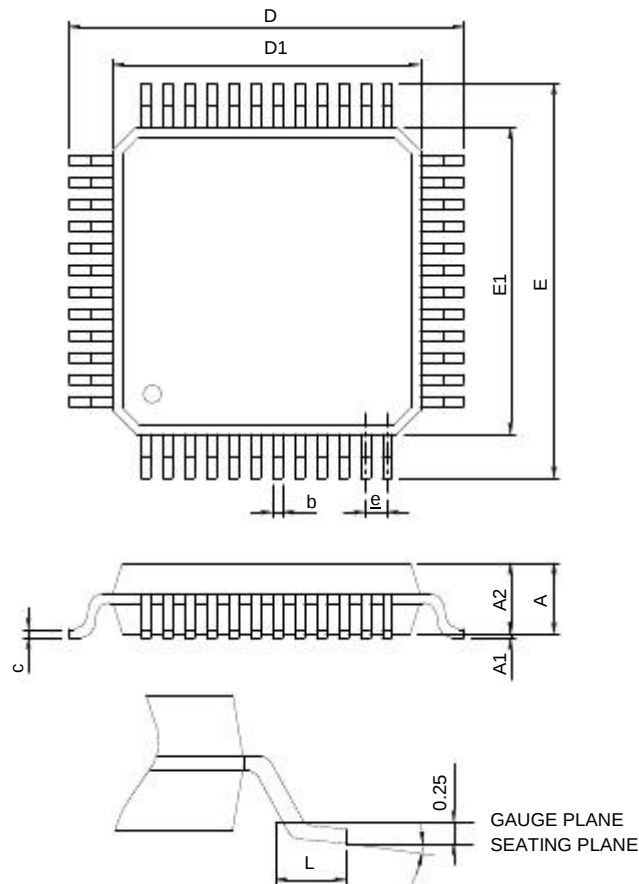


where VREF is the output of the reference voltage (2.49V typical) at VREF pin. The amplitude of the triangular waves CT1 and CT2 are typically 0.7V from 1.1V to 1.8V.

JTMA7095/A

Package Information

LQFP7x7-48



SYMBOL	LQFP7x7-48			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.60		0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.17	0.27	0.007	0.011
c	0.09	0.20	0.004	0.008
D	8.80	9.20	0.346	0.362
D1	6.90	7.10	0.272	0.280
E	8.80	9.20	0.346	0.362
E1	6.90	7.10	0.272	0.280
e	0.50 BSC		0.020 BSC	
L	0.45	0.75	0.018	0.030
0	0°	7°	0°	7°

Note : 1. Followed from JEDEC MS-026 BBC.

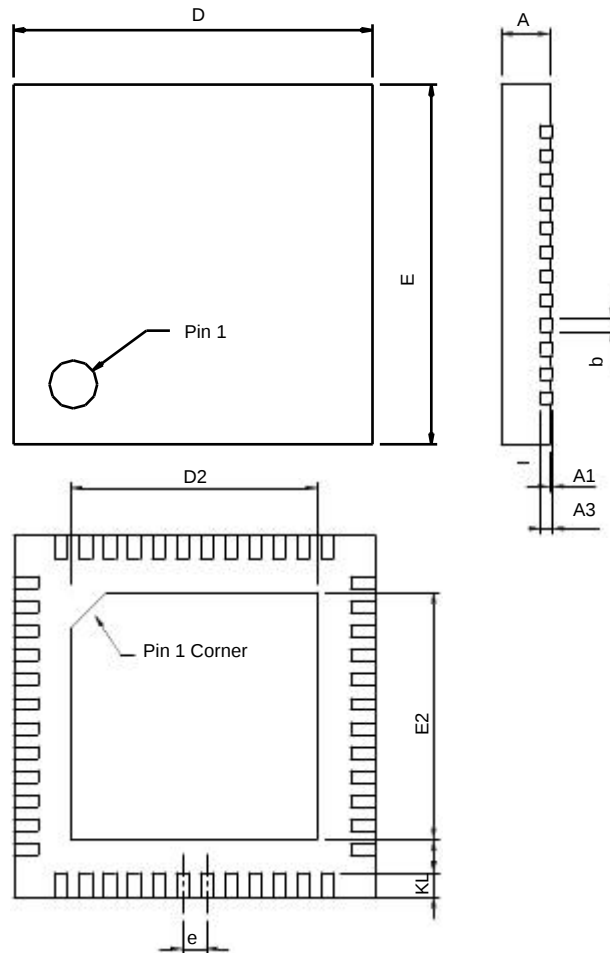
2. Dimension "D1" and "E1" do not include mold protrusions.

Allowable protrusions is 0.25 mm per side. "D1" and "E1" are maximum plasticbody size dimensions including mold mismatch.

JTMA7095/A

Package Information

TQFN7x7-48



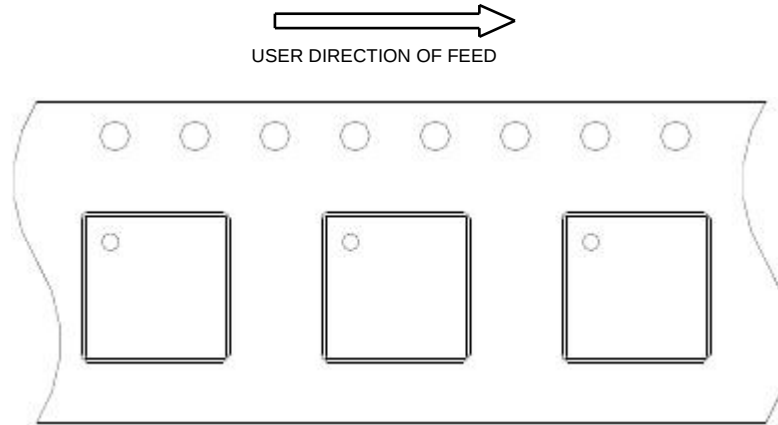
S Y M B O L	TQFN7x7-48			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	6.90	7.10	0.272	0.280
D2	5.50	5.80	0.217	0.228
E	6.90	7.10	0.272	0.280
E2	5.50	5.80	0.217	0.228
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-220 WKD-4.

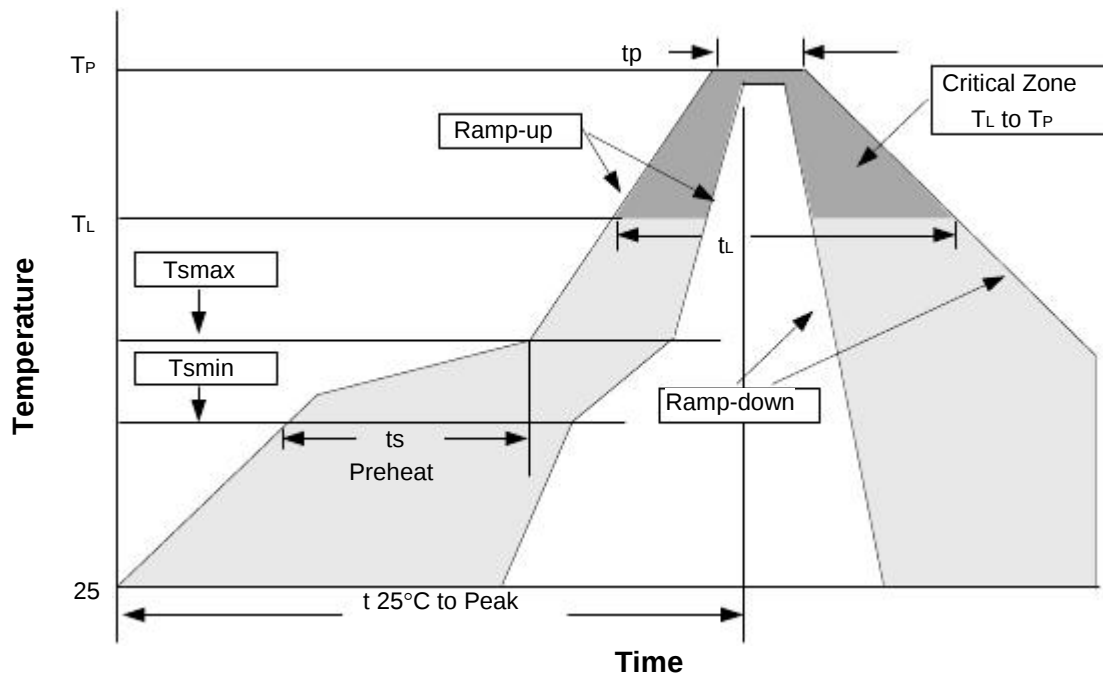
JTMA7095/A

Taping Direction Information

(T)QFN7x7



Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B, A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, $I_{tr} > 100mA$

JTMA7095/A

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T _L to T _P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (T _{smin}) - Temperature Max (T _{smax}) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T _L) - Time (t _L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classification Temperature (T _p)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Note: All temperatures refer to topside of the package. Measured on the body surface.

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm ³ <350	Volume mm ³ ε350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
ε2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
ε2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

Customer Service