JTMA7116

3-in-1 Dual PWM Buck and Linear DDR Power Controller

Features

- **Provide Synchronous Rectified Buck PWM Controllers for VDDQ and VMCH**
- **Integrated Power FETs with VTT Regulator Source/Sink up to 2.0A**
- **Drive Low Cost N-Channel Power MOSFETs**
- **Internal 0.8V Reference Voltage for Adjustable VDDQ and VMCH**
- **Thermal Shutdown**
- **VTT Tracks at Half the Reference Voltage**
- **Fixed Switching Frequency of 250kHz for VDDQ and VMCH**
- **Over-Current Protection and Under-Voltage Protection for VDDQ and VMCH**
- **Fully Complies with ACPI Power Sequencing Specifications**
- **180 degrees Phase Shift between VDDQ and VMCH**
- **Power-OK Function for VDDQ and VMCH**
- **Fast Transient Response**
  - **Maximum Duty Cycle 90%**
  - **High-Bandwidth Error Amplifier**
- **Simple Single-Loop Control Design**
  - **Voltage Mode PWM Control**
  - **External Compensation**
- **External Soft-Start for VDDQ and VMCH**
- **Shutdown Function for VDDQ/VTT and VMCH**
- **Thermally Enhanced TSSOP-24P Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **DDR Memory and MCH Power Supply**

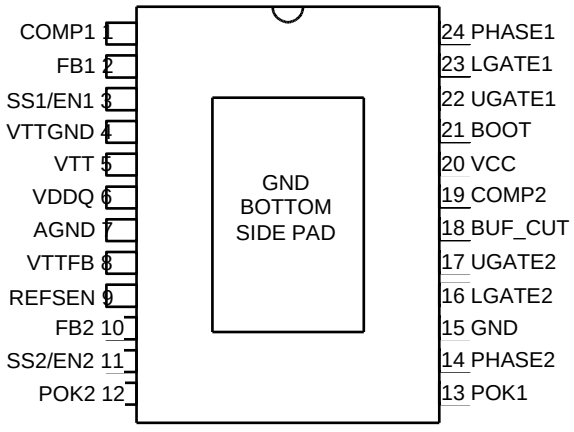
General Description

The JTMA7116 integrates Dual PWM buck controllers and an internal linear regulator for DDR memory and MCH power solution. The two synchronous PWM buck controllers drive four N-channel MOSFETs for DDR memory supply voltage (VDDQ) and MCH regulator. The internal regulator is designed to track at the half of the reference voltage with sourcing and sinking current for DDR memory termination regulator (VTT).

The JTMA7116 uses the latched BUF_Cut signal and the POR of the BOOT to comply with ACPI power sequencing specifications. The two PWM regulators also provide POK signals to indicate that the regulators are good. The device also has the phase shift function between the two PWM controllers. The protection functions of the two PWM controllers include over-current protection, under-voltage protection, and external soft-start function. The VTT regulator provides 2A sinking and sourcing current-limit function and also has thermal shutdown protection.

The TSSOP-24P package with a copper pad provides excellent thermal impedance is available.

Pin Configuration



TSSOP-24P
(TOP VIEW)

Ordering and Marking Information

JTMA7116 □□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code R : TSSOP-24P Operating Ambient Temperature Range E : - 20 to 70 C° Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
JTMA7116 R : JTMA7116 XXXXX	XXXXX - Date Code

Note: JTMA lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. JTMA lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. JTMA defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{CC}	VCC to AGND	-0.3 to 6	V
V_{BOOT}	BOOT to AGND	-0.3 to 14	V
UGate Drive	UGATE1, UGATE2 to GND DC Voltage <100ns Pulse Width	-0.3 to VBOOT+0.3 -4 to VBOOT+2	V
LGate Drive	LGATE1, LGATE2 to GND DC Voltage <100ns Pulse Width	-0.3 to VCC+0.3 -4 to VCC +2	V
PHASE	PHASE1, PHASE2 to GND DC Voltage <100ns Pulse Width	-0.3 to 14 -4 to 16	
V_{IO}	Input/Output Pins to AGND Pins 1-3, 5-6, 8-14, 18-19, 24	-0.3 to 14	V
I_{VTT}	VTT Output Current	+/-2A	A
GND	GND, VTTGND to AGND	-0.3 to +0.3	V
T_J	Maximum Junction Temperature	+150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Soldering Temperature, 10 Seconds	260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Range			Unit
		Min.	Typ.	Max.	
V_{CC}	VCC to AGND	4.5	5	5.5	V
V_{BOOT}	BOOT to AGND	10.8	12	13.2	V
V_{IN}	Power Input Voltage of PWM Controllers to AGND	2.97	5	5.5	V
V_{DDQ}	VDDQ to AGND	0.8	-	2.5	V
V_{MCH}	VMCH to AGND	0.8	-	1.5	V
V_{REFSEN}	V_{REFSEN} to AGND	1.8	-	2.5	V

Recommended Operating Conditions (Cont.)

Symbol	Parameter	Range			Unit
		Min.	Typ.	Max.	
I_{VTT}	VTT Output Current	-1.8	-	1.8	A
T_J	Operating Junction Temperature	-20	-	125	°C
T_A	Operating Ambient Temperature	-20	-	70	°C

Electrical Characteristics

Operating Conditions: V_{CC}=5V, BOOT=12V, T_A = -20°C to 70°C, unless Otherwise Specified.

Symbol	Parameter	Test Conditions	JTMA7116			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{VCC}	VCC supply Current (S0 Mode)	S0 Mode, UGATEs, LGATEs open	-	5	10	mA
	VCC supply Current (S3 Mode)	S3 Mode, UGATEs, LGATEs open	-	2.5	5	mA
	VCC supply Current (S5 Mode)	S5 Mode, UGATEs, LGATEs open	-	0.5	1.0	mA
I_{BOOT}	BOOT supply Current (S0 Mode)	S0 Mode, UGATEs, LGATEs are switching	-	1.5	5	mA
	BOOT supply Current (S3 Mode)	S3 Mode, UGATEs, LGATEs are switching	-	1	5	mA
POWER-ON-RESET THRESHOLD						
V_{CC}	VCC Power-On-Reset Threshold	VCC Rising	4.0	4.2	4.4	V
		VCC Falling	3.8	3.9	4.0	V
V_{BOOT}	BOOT Power-On-Reset Threshold	VBOOT Rising	10.0	10.2	10.4	V
		VBOOT Falling	9.1	9.3	9.5	V
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown	(Note2)	-	150	-	°C
T_{SDHYS}	Thermal Shutdown Hysteresis	(Note2)	-	50	-	°C
OSCILLATOR (PWM1 AND PWM2)						
F_{OSC}	Oscillator Frequency		225	250	275	kHz
□V_{OSC}	Oscillator Ramp Amplitude	(Note2)	-	1.9	-	V
Duty	Duty Cycle Range (Note2)		0	-	90	%
REFERENCE VOLTAGE						
V_{REF1}	Reference Voltage		-	0.8	-	V
	Reference Voltage Accuracy		-1.0	-	+1.0	%
	Load Regulation	I_{VDDQ} = 0 to 10A	-	0.2	-	%
V_{REF2}	Reference Voltage		-	0.8	-	V
	Reference Voltage Accuracy		-1.0	-	+1.0	%
	Load Regulation	I_{GMCH} = 0 to 5A	-	0.2	-	%
POWER-OKAY (POK1 AND POK2)						
V_{POKLT}	Low Threshold	FB Falls % of V_{REF}	83	-	-	%
V_{POKHT}	High Threshold	FB Reaches % of V_{REF}	-	-	90	%
I_{LKG}	Leakage Current	V_{POK} = 5V	-	-	1	∝A
V_{POKOL}	POK Low Voltage	I_{POK} = 2mA	-	0.16	0.3	V

Electrical Characteristics (Cont.)

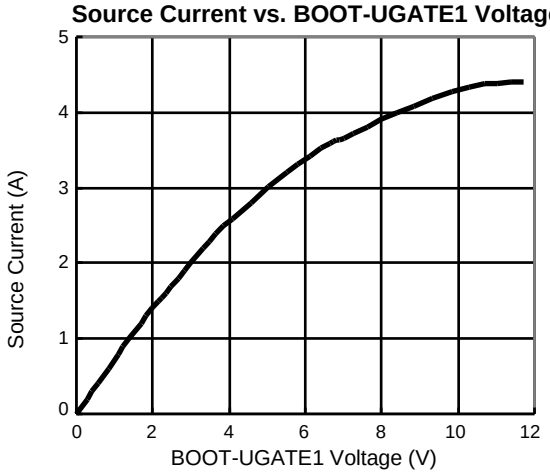
Operating Conditions: V_{CC}=5V, BOOT=12V, T_A = -20°C to 70°C, unless Otherwise Specified.

Symbol	Parameter	Test Conditions	JTMA7116			Unit
			Min.	Typ.	Max.	
ERROR AMPLIFIER (PWM1 AND PWM2)						
	Open Loop Gain (Note2)	R_L=10k& to GND	-	75	-	dB
	Open Loop Bandwidth (Note2)	R_L=10k& to GND, C_L=100pF	-	12	-	MHz
	Slew Rate (Note2)	R_L=10k& to GND, C_L=100pF	-	8	-	V/∝s
	Output High Source Current	COMP = 2.5V	-	40	-	mA
	Output Low Sink Current	COMP = 2.5V	-	40	-	mA
PROTECTION AND MONITOR (PWM1 AND PWM2)						
I_{OCSET}	PHASE Source Current		90	110	130	∝A
V_{OCP}	OCP Reference Voltage		0.17	0.2	0.23	V
	FB Under Voltage Level	Output Falls % of V_{REF}	55	60	65	%
I_{SS}	Soft-Start Charge Current		8	11	14	∝A
	SS/EN Shutdown Threshold		-	-	0.2	V
VTT REGULATOR						
VTT	VTT Output Voltage	I_{OUT} = -10mA to 10mA V_{REFSEN}= 2.5V	-20	-	20	mV
		I_{OUT} = -10mA to 10mA V_{REFSEN}= 1.8V	-13	-	-13	mV
	Load Regulation	I_{OUT} = -2A to 2A	-1	-	1	%
	Line Regulation	VDDQ = 1.8V to 2.5V	-	-	0.2	%
R_{REFSEN}	REFSEN Input Resistance	(Note2)	-	50	-	k&
	VTTFB Hysteresis (Note2)	% of REFSEN	-	0.1	-	%
ILIMVTT	VTT Source Current Limit		2	2.5	3	A
	VTT Sink Current Limit		2	2.5	3	A
$R_{DS(ON)}$	Internal Power FETs $R_{DS(ON)}$		-	0.3	0.4	&
	Internal Soft-Start Interval	(Note2)	-	0.5	-	ms
BUF_CUT CONTROL						
V_{BUF_CUTH}	BUF_CUT Input Logic High		2.0	-	-	V
V_{BUF_CUTL}	BUF_CUT Input Logic Low		-	-	0.8	V
I_{BUF_CUT}	BUF_CUT Input Current		1	3	5	∝A
GATE DRIVERS						
	UGATE1 Source	BOOT=12V, UGATE1=2V	1	1.5	-	A
	UGATE1 Sink	VCC=5V, UGATE1=2V	-	1.2	1.8	&
	LGATE1 Source	BOOT=12V, LGATE1=2V	1.7	2.5	-	A
	LGATE1 Sink	VCC=5V, LGATE1=2V	-	0.45	0.675	&
	UGATE2 Source	BOOT=12V, UGATE2=2V	0.7	1	-	A
	UGATE2 Sink	VCC=5V, UGATE2=2V	-	2.3	3.45	&
	LGATE2 Source	BOOT=12V, LGATE2=2V	1.3	1.9	-	A
	LGATE2 Sink	VCC=5V, LGATE2=2V	-	0.6	0.9	&
	Dead Time (Note2)		-	20	-	ns

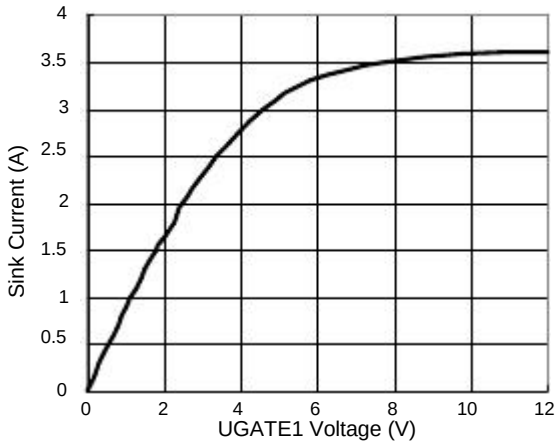
Note 2: Guaranteed by design, not tested in production.

Typical Operating Characteristics

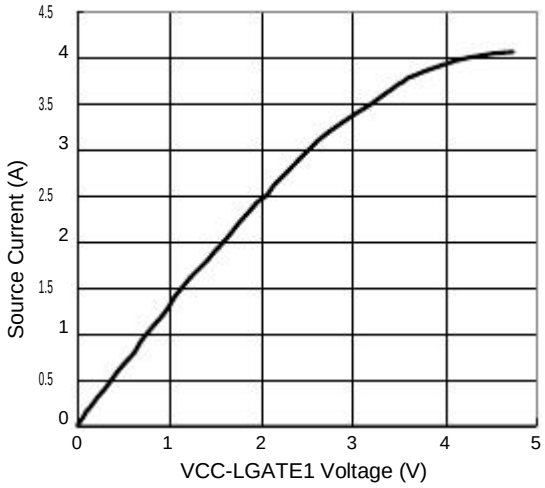
Source Current vs. BOOT-UGATE1 Voltage



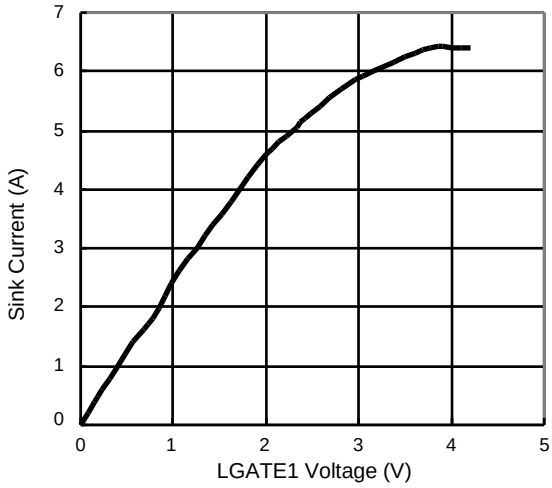
Sink Current vs. UGATE1 Voltage



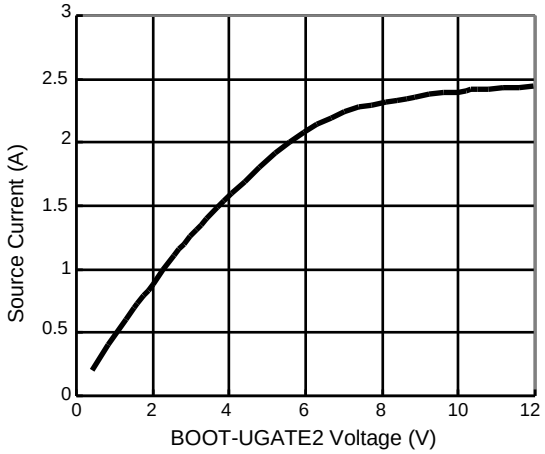
Source Current vs. VCC-LGATE1 Voltage



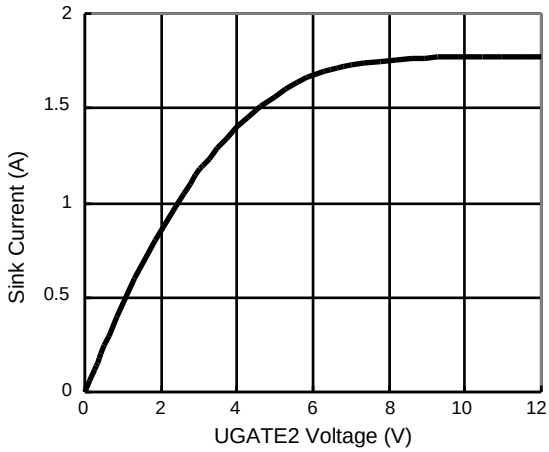
Sink Current vs. LGATE1 Voltage



Source Current vs. BOOT-UGATE2 Voltage

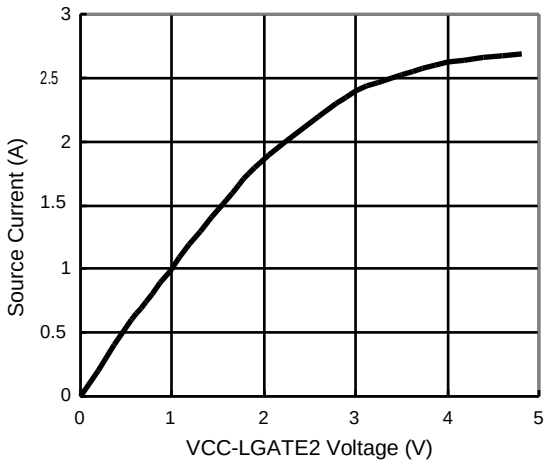


Sink Current vs. UGATE2 Voltage

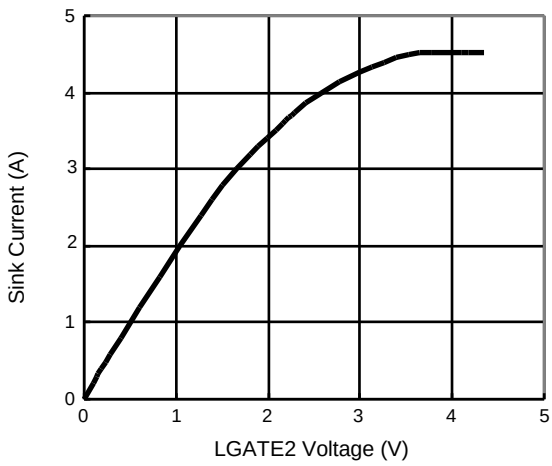


Typical Operating Characteristics (Cont.)

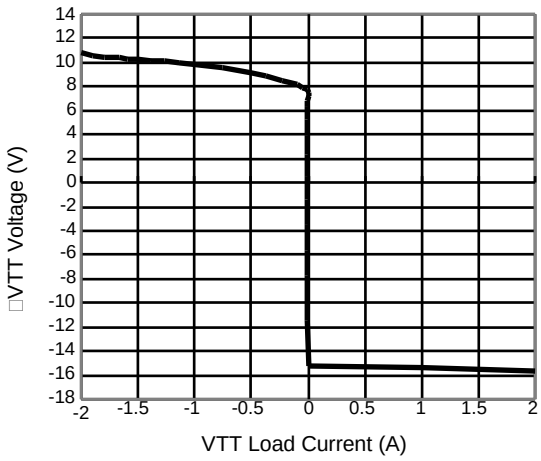
Source Current vs. VCC-LGATE2 Voltage



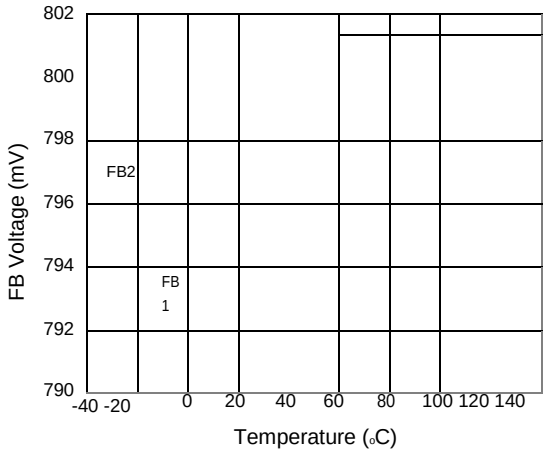
Sink Current vs. LGATE2 Voltage



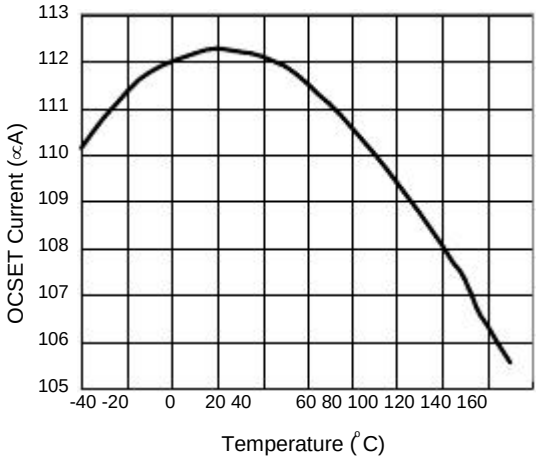
□VTT Voltage vs. VTT Load Current



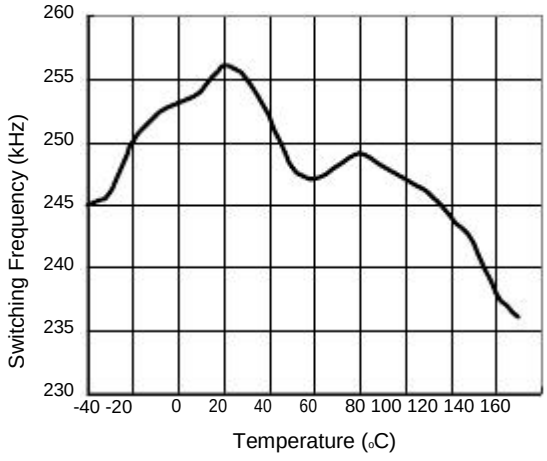
FB Voltage vs. Temperature



OCSET Current vs. Temperature

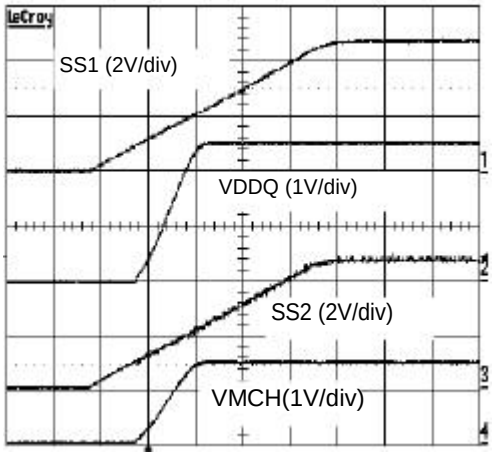


Switching Frequency vs. Temperature



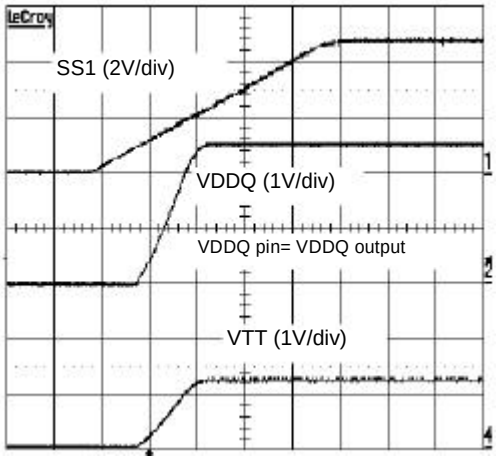
Typical Operating Characteristics (Cont.)

VDDQ & VMCH Power Up



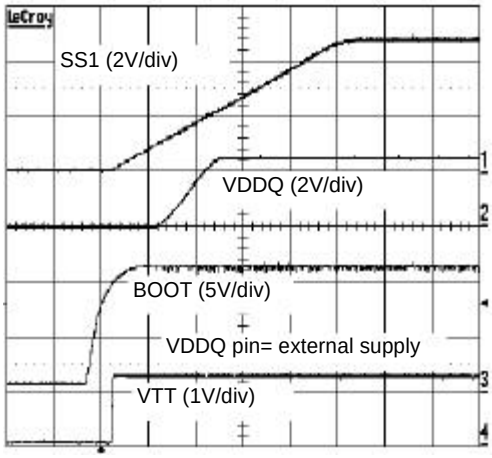
Time (10ms/div)

VDDQ & VTT Power Up1



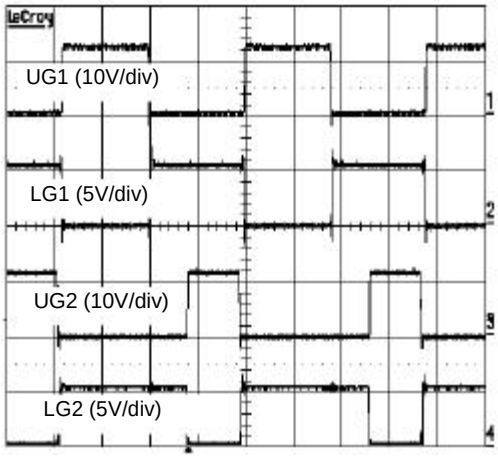
Time (10ms/div)

VDDQ & VTT Power Up2



Time (10ms/div)

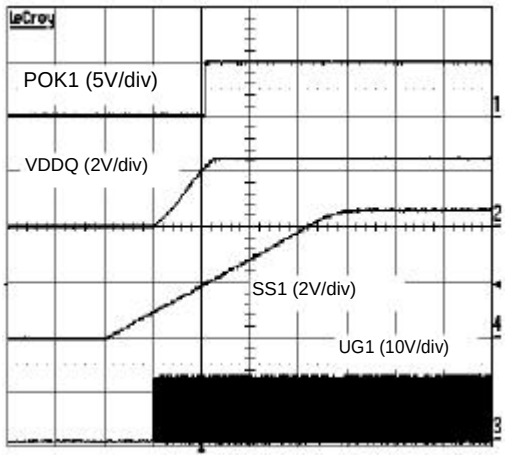
Phase Shift



Time (1∝s/div)

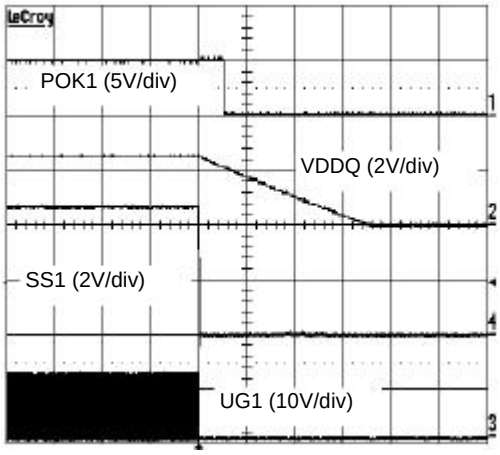
Typical Operating Characteristics (Cont.)

Enable VDDQ



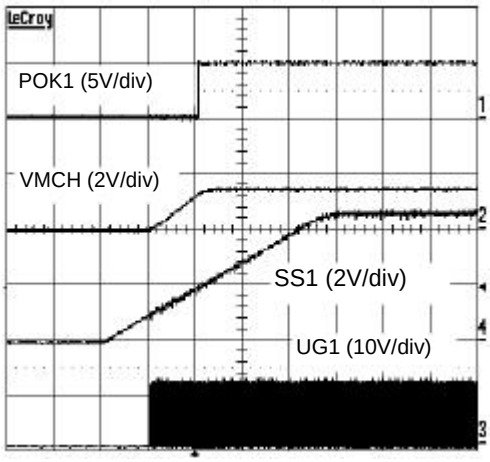
Time (10ms/div)

Disable VDDQ



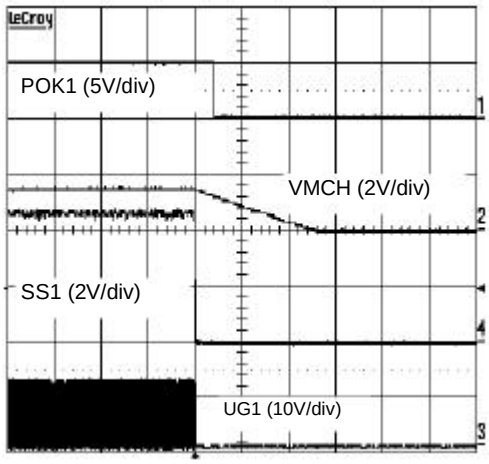
Time (10ms/div)

Enable VMCH



Time (10ms/div)

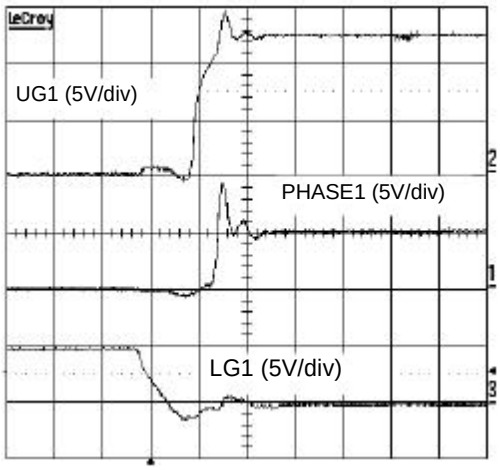
Disable VMCH



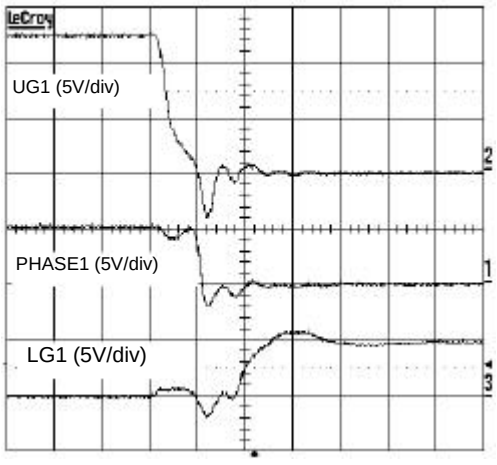
Time (10ms/div)

Typical Operating Characteristics (Cont.)

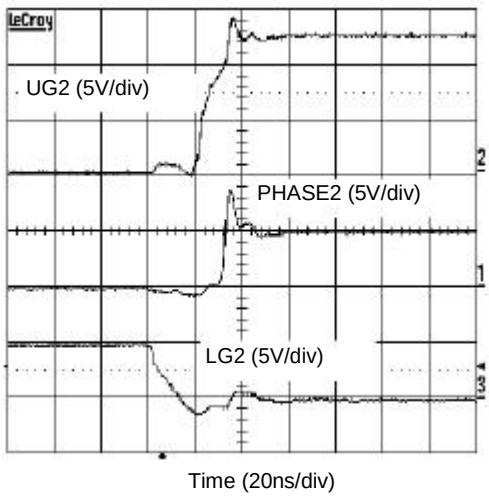
UG1 Rising



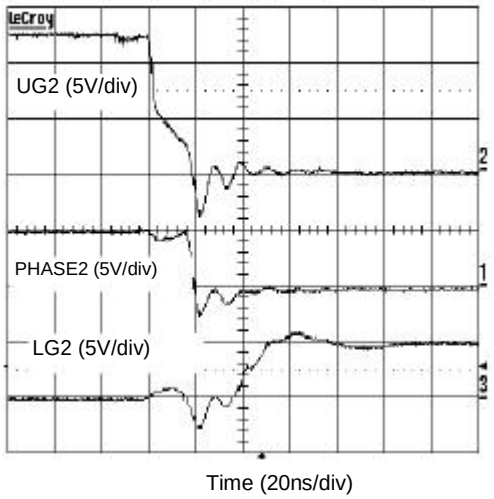
UG1 Falling



UG2 Rising

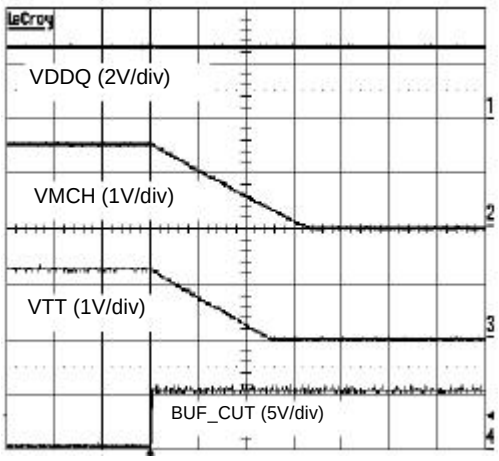


UG2 Falling



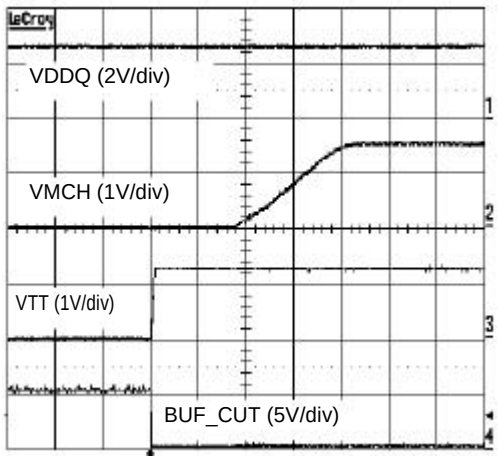
Typical Operating Characteristics (Cont.)

S0 to S3



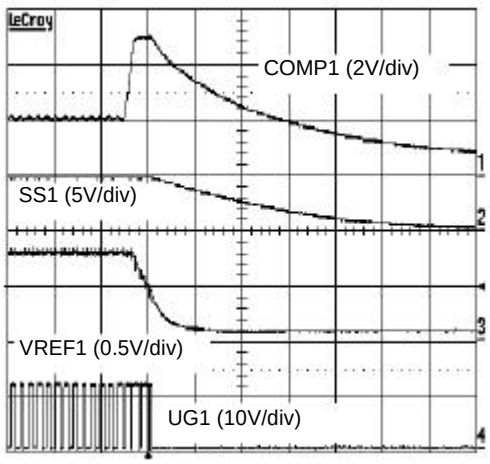
Time (5ms/div)

S3 to S0



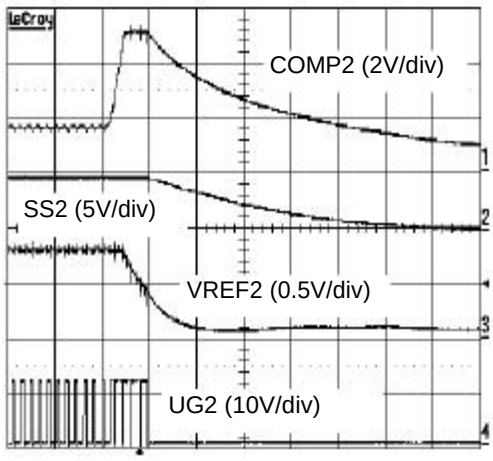
Time (5ms/div)

VDDQ UVP



Time (20∝s/div)

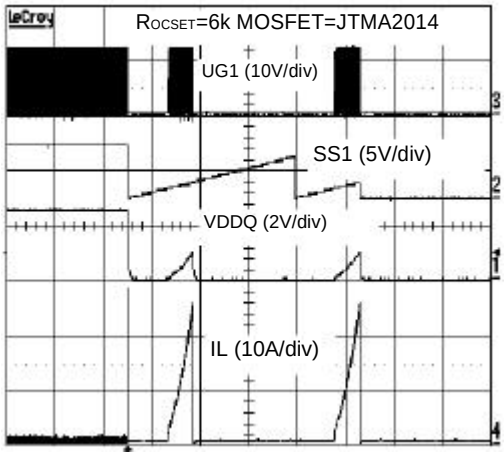
VMCH UVP



Time (20∝s/div)

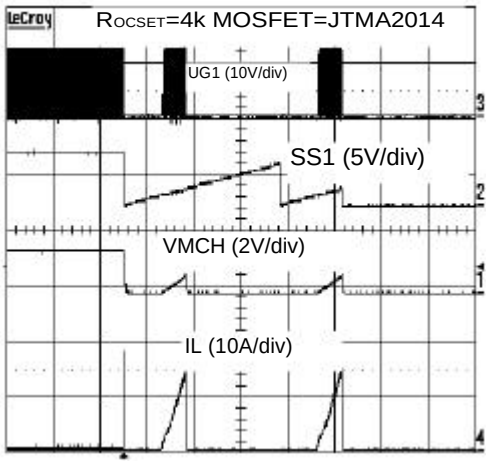
Typical Operating Characteristics (Cont.)

VDDQ OCP



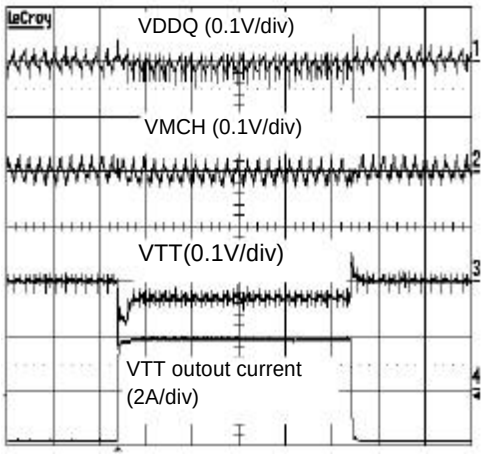
Time (10ms/div)

VMCH OCP



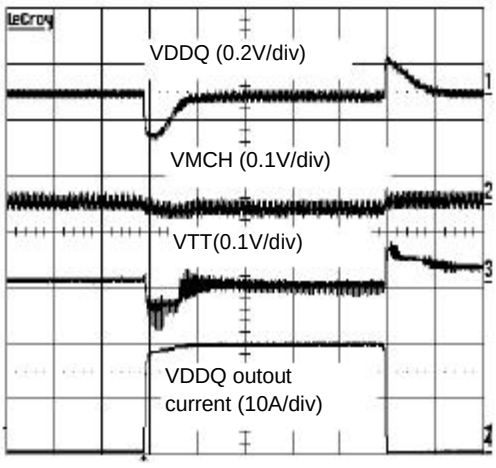
Time (10ms/div)

VTT Load Transient



Time (20∝s/div)

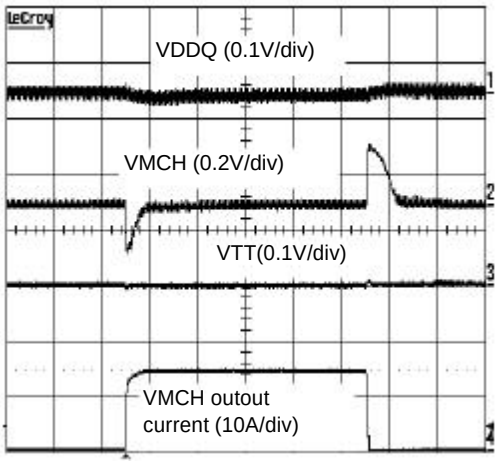
VDDQ Load Transient



Time (0.1ms/div)

Typical Operating Characteristics (Cont.)

VMCH Load Transient



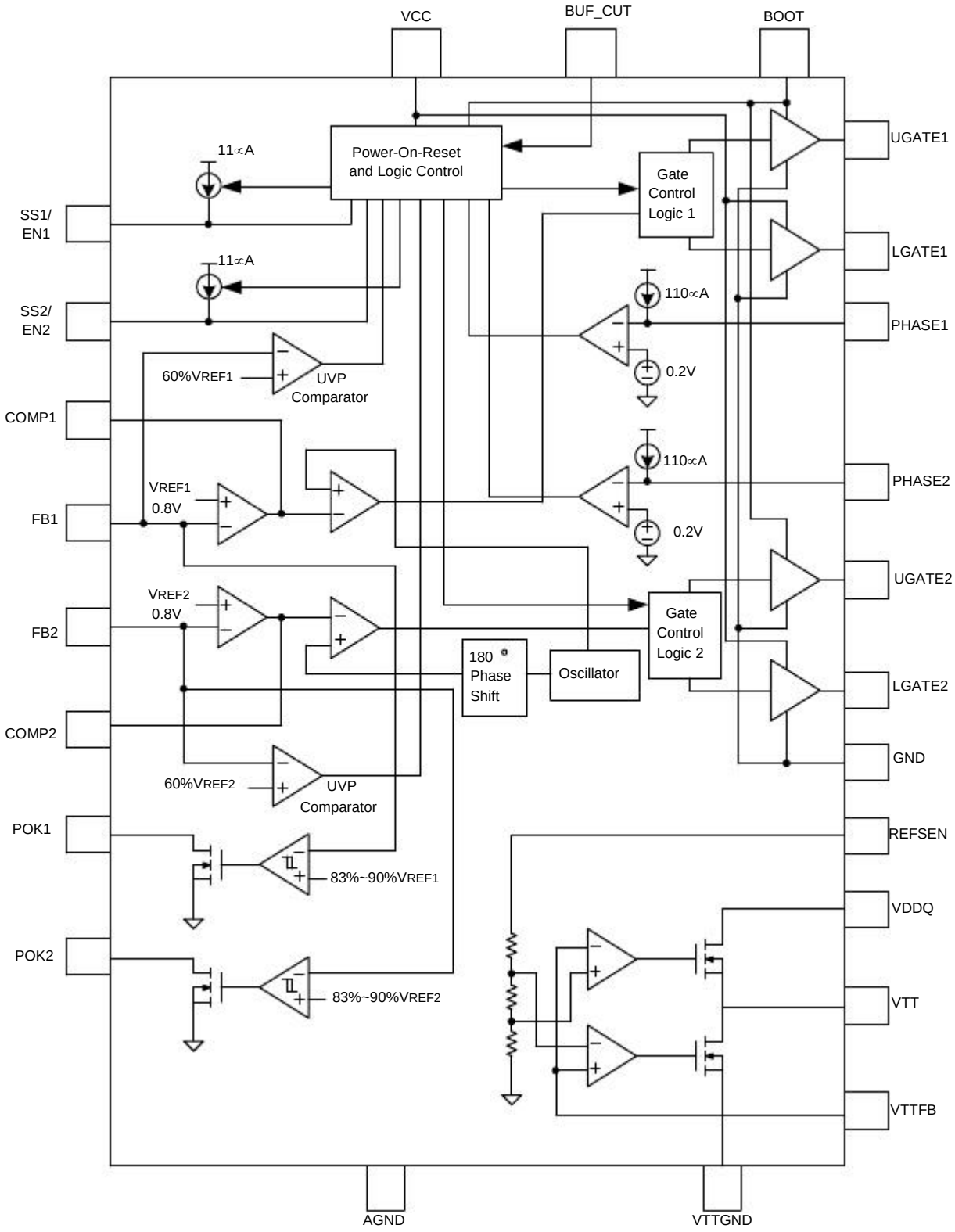
Pin Description

PIN		FUNCTION
NO.	NAME	
1	COMP1	These pins are the output of error amplifiers of their respective regulators. They are used to set the compensation components.
2	FB1	These pins are the inverting input of the error amplifiers of their respective regulators. They are used to set the output voltage and the compensation components. If the FB voltage is under 60% of reference voltage,
3	SS1	Connect a capacitor to the GND for setting the soft-start time. Use an open drain logic signal to pull the SS/EN pin low to disable the respective output, leave open to enable the respective output.
4	VTTGND	VTT return. Connect to copper plane carrying VTT return current. The trace connecting to this pin must be able to carry 2A.
5	VTT	VTT regulator output.
6	VDDQ	Power input for VTT regulator.
7	AGND	Analog ground. Compensation Components and the Soft-Start capacitors connect to this ground.
8	VTTFB	VTT regulation pin for closed loop regulation.
9	REFSEN	Reference voltage input of VTT regulator. VTT will be regulated to 1/2 of this voltage. Connect to point of load.
10	FB2	These pins are the inverting input of the error amplifiers of their respective regulators. They are used to set the output voltage and the compensation components. If the FB voltage is under 60% of reference voltage,
11	SS2	Connect a capacitor to the GND for setting the soft-start time. Use an open drain logic signal to pull the SS/EN pin low to disable the respective output, leave open to enable the respective output.

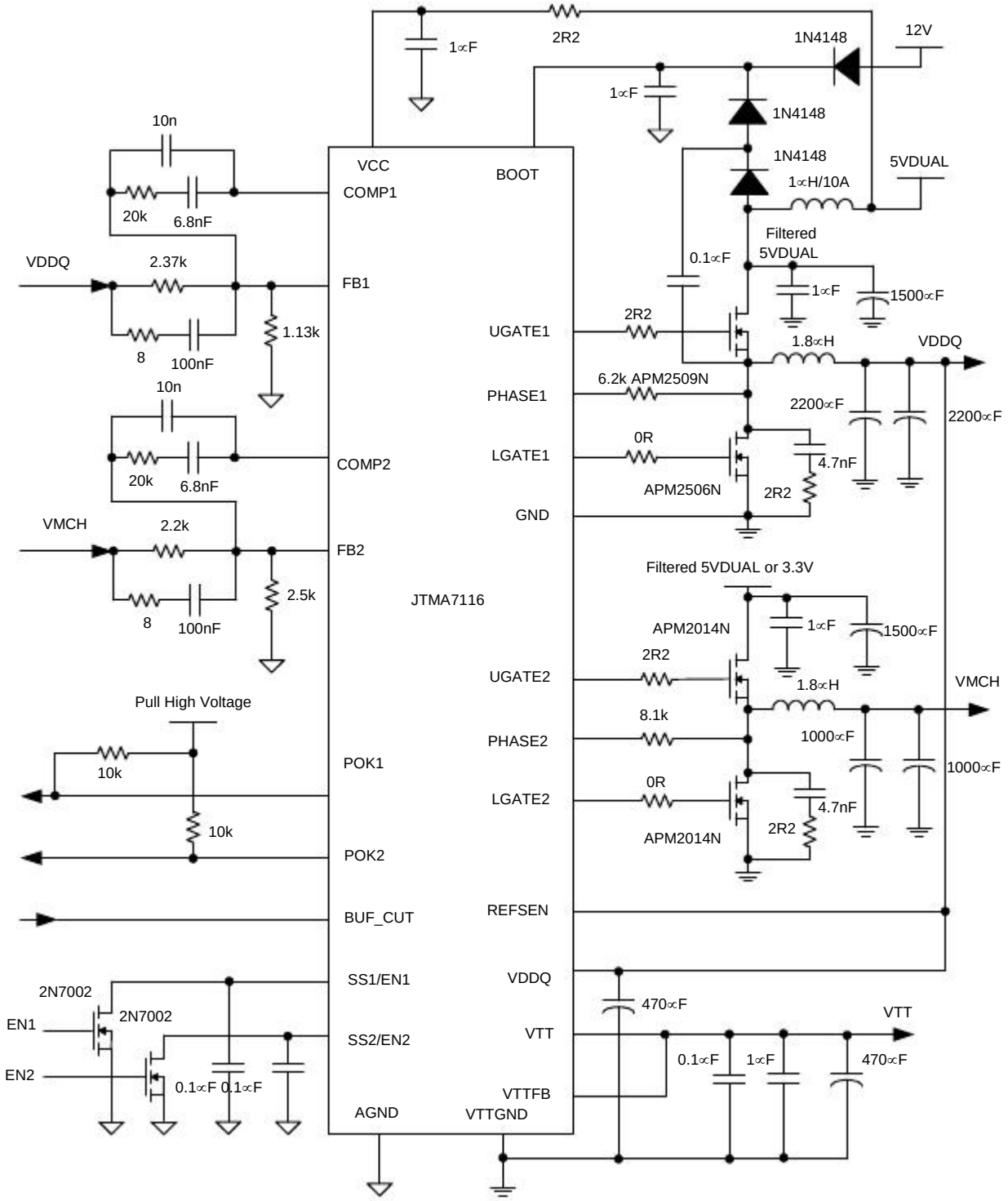
Pin Description (Cont.)

PIN		FUNCTION
NO.	NAME	
12	POK2	These pins are open-drain pull-down devices. When respective FB falls 83% of reference voltage, the output is pulled low. When respective FB reaches 90% reference voltage, the output is pulled high, for power is okay.
13	POK1	These pins are open-drain pull-down devices. When respective FB falls 83% of reference voltage, the output is pulled low. When respective FB reaches 90% reference voltage, the output is pulled high, for power is okay.
14	PHASE	A resistor (ROCSET) is connected between this pin and the drain of the low-side MOSFET will determine the over current limit of PWM converter.
15	GND	This pin is the power ground pin for the gate drivers.
16, 23	LGATE	These pins provide the gate drivers for the lower MOSFETs of VDDQ and VMCH.
17	UGATE2	These pins provide the gate drivers for the upper MOSFETs of VDDQ and VMCH.
18	BUF_CUT	Active high control signal to activate S3 sleep state. BUF_CUT is pulled low by internal 3∝A current
19	COMP2	These pins are the output of error amplifiers of their respective regulators. They are used to set the compensation components.
20	VCC	Power supply input pin. Connect a nominal 5V power supply to this pin for control circuit and lower gate drivers.
21	BOOT	Upper gate drivers input supply.
22	UGATE1	These pins provide the gate drivers for the upper MOSFETs of VDDQ and VMCH.
24	PHASE1	A resistor (ROCSET) is connected between this pin and the drain of the low-side MOSFET will determine the over current limit of PWM converter.

Block Diagram



Typical Application Circuit



Function Description

Soft-Start/Enable

The VDDQ and VMCH regulators have independent soft-start control and shundown function. Connect a capacitor from each SS pin to the GND to set the soft-start interval of the VDDQ and VMCH and an open drain logic signal for each SS/EN pin to enable or disable the respective output. Figure1 shows the soft-start interval. At t0, the VCC and Boot voltoge are above their POR trip points, a 11∝A current source starts to charge the capacitor and the VTT starts it's internal soft-start interval. The soft-start interval of VTT is about 500∝s. When the SS reaches 1V, the internal reference voltage starts to rise and follows the SS. Until the SS reaches about 2V at t3, the internal reference completes the soft-start interval and reaches to 0.8V. The soft-start of VMCH is the same as the VDDQ. This method provides a rapid and controlled output voltage rise.

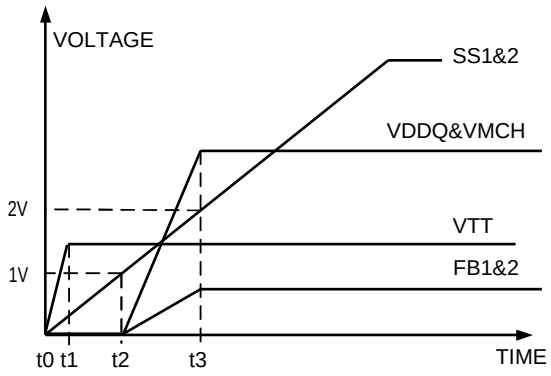


Figure 1. Soft-Start Interval

$$t_{SS} = t3 - t2 = \frac{C_{SS} \cdot 1V}{I_{SS}\ (11uA)}$$

$$t1 - t0 = 0.5ms$$

Where: C_{SS} = External Soft-Start capacitor

I_{SS} = Soft-Start charg current

Power-Okay

The Power-Okay function monitors the VDDQ and VMCH and drives low to indicate a fault. When a fault condition, such as over-current, short-circuit, thermal shutdown is occurred, and the VDDQ or VMCH falls to 83% of it's nominal voltage, the POK is pulled low. When the VDDQ or VMCH reaches to 90% of it's nominal voltage, the POK is pulled high. Since the POK is an open-drain device, connecting a 10k& resistor to a pull high voltage is necessary.

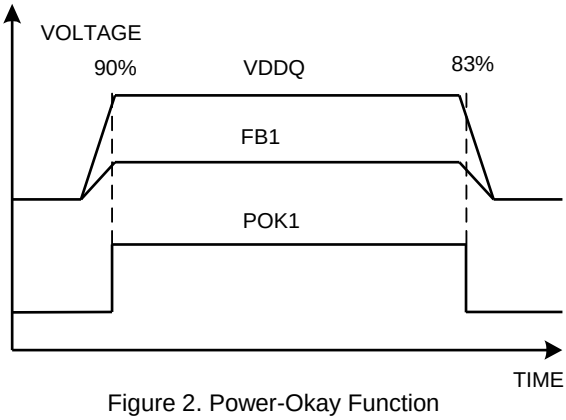


Figure 2. Power-Okay Function

Over-Current Protection

A resistor (ROCSET) is connected between the phase pin and the drain of the low-side MOSFET will determine the over-current limit. An internally generated 110∝A current source will flow through this resistor, creating a voltage drop. When the volatge across the low-side MOSFET exceeds the voltage across the ROCSET minus V_{OCP} , the OCP is detected. The OCP function will trip at a peak inductor current, the threshold of the over-current limit is therefore given by:

$$I_{LIMIT} = \frac{R_{OCSET} \cdot I_{OCSET} - V_{OCP}}{R_{DS(ON)} \text{ of the lower MOSFET}}$$

For the over-current is never occurred in the normal operating load range; the variation of all parameters in the above equation should be determined.

- The MOSFET $R_{DS(ON)}$ is varied by temperature and gate to source voltage, the user should determine the maximum $R_{DS(ON)}$ in manufacturer's datasheet.
- The minimum I_{OCSET} (90∝A), maximum Vocp (230mV) and minimum R_{OCSET} should be used in the above equation. Use 1% or better resistor for R_{OCSET} is recommended.
- Note that the ILIMIT is the current flow through the upper MOSFET; ILIMIT must be greater than maximum output current add the half of inductor ripple current.

An over-current condition will repeat the soft-start function 3 times ; if the over-current condition is not removed during the 3 times soft-star interval, and then all regulators will be shut down, and require a POR on either of VCC or VBOOT to restart IC.

Function Description (Cont.)

Over-Current Protection (Cont.)

Note that the parastic capacitor from PHASE pin to the GND will distort the PHASE pin signal and the current limit will be larger than set value. Reduce the parastic capacitance as small as possible to make the current limit meet set value.

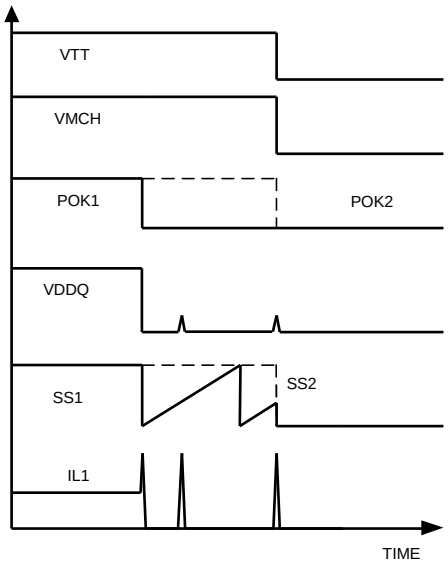


Figure 3. VDDQ Over-Current Protection Waveforms

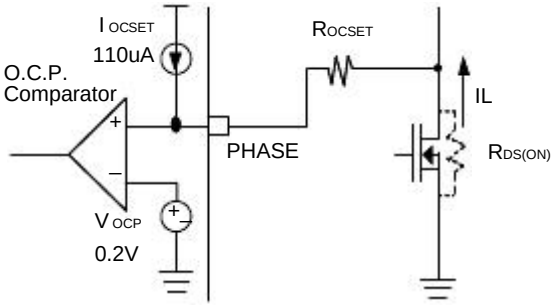


Figure 4. Low-side Over-Current Protection Circuit

VTT Regulator

The VTT regulator has two internal N-Channel FETs to provide current sink and source capability up to 2A. The VTT regulator is tracked at the half of REFSEN voltage by the internal resistor divider. When both VCC and BOOT voltages reach their rising POR trip points, the soft-start of the VTT starts rising; the soft-start interval is about 0.5ms. The VTT regulator is activated only in S0 mode; in S3 mode, the VTT regulator is not needed and turned off.

The VTT regulator has 2.5A sink and source current limit to protect the internal FETs. When current limit is occurred, the regulator keeps the load current at 2.5A. The device provides a soft-start function when current limit condition is released.

Phase Shift

The JTMA7116 has phase shift function between the two PWM converters. The phase difference is relative to the falling edges of UGATE1 and UGATE2 and the phase shift is fixed at 180 degrees (see figure 5). However, the phase shift between the rising edge of UGATE1 and UGATE2 , depending on the duty cycles, the rising edges might overlap, therefore, the user should check it.
The advantage of phase shift is to avoid overlapping the switching current spikes of the two channels, or interaction between the channels; it also reduces the RMS current of the input capacitors, allowing fewer caps to be employed.

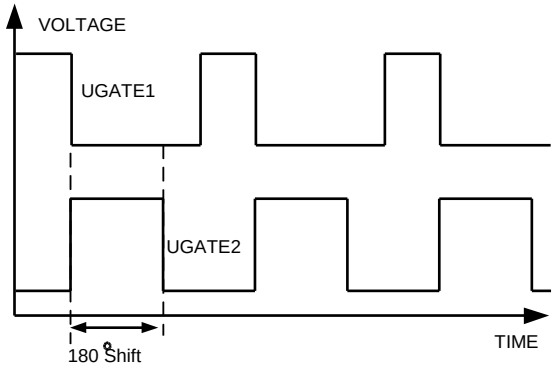


Figure 5. Phase of UG2 with respect to falling edge of UG1

Thermal Shutdown

When the junction temperature exceeds 150 °C, the device shut down to protect the device from damage. After the temperature decreases to 100 °C, the device starts up again.

ACPI Control Logic

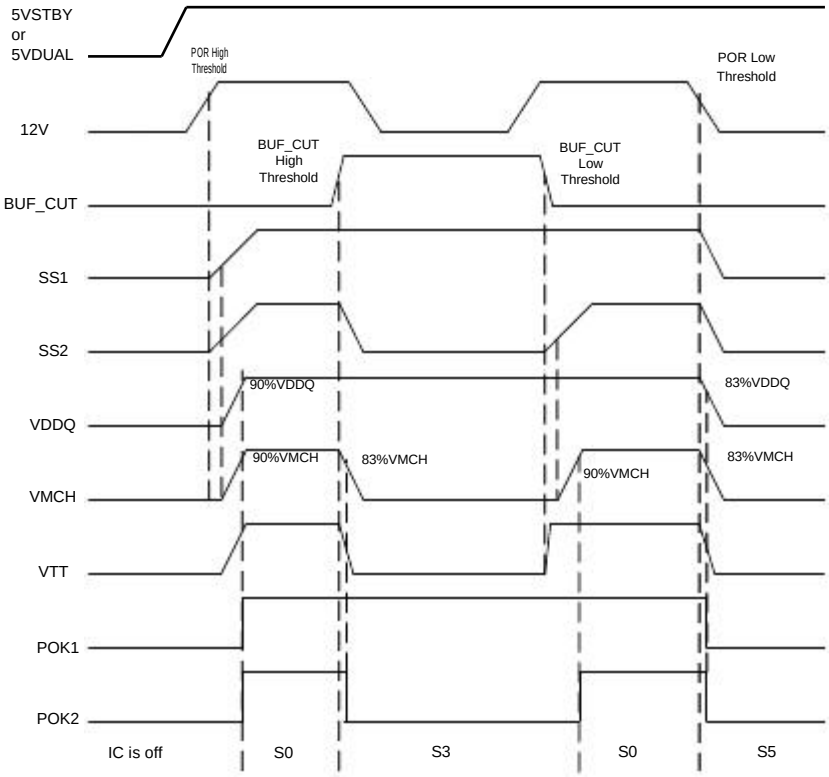
The BUF_CUT signal and two Power-On-Reset thresholds on VCC and BOOT pins are used to determine the operating mode. The VCC and BOOT are supplied by external supplies 5VDUAL and 12VATX. When the VCC

Function Description (Cont.)

ACPI Control Logic (Cont.)

and BOOT voltage are above their POR rising trip points, the device is enabled and enters the S0 normal operating mode. The BUF_CUT is pulled low by internal current source. Pull the BUF_CUT to high in S0 mode, the device enters the S3 sleep mode. In S3 mode, the output voltages VTT and VMCH are disabled and supply voltage 12VATX is not supplied to the device. When BUF_CUT is pulled low and the 12VATX is enabled, the operating mode will be back to S0 mode. If the 12VATX supply voltage is removed, the device is into S5 shutdown mode, all regulator will be shut down. Note that transition from S3 to S5 is not allowed. A timing diagram is shown in Figure 6 and a state transitions diagram is shown in Figure 7.

Function Description (Cont.)



Figur 6. ACPI Timing Diagram

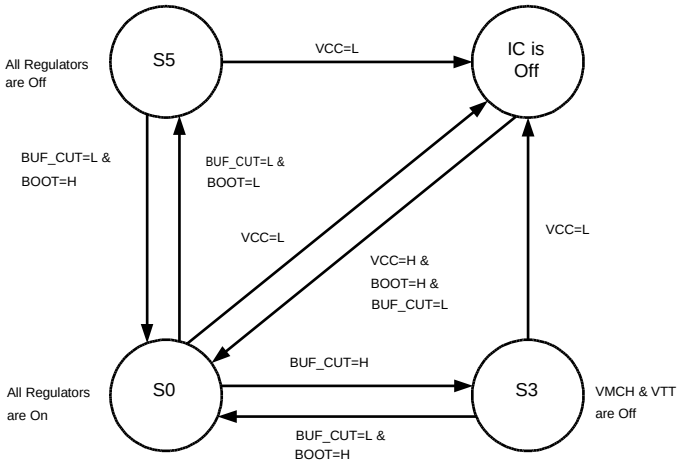


Figure 7. State Transitions Diagram

Application Information

Output Voltage Setting

The output voltage of the PWM converter can be adjusted with a resistive divider. The internal reference voltage is 0.8V. The following equation can be used to calculate the output voltage:

$$VOUT = (1+ \frac{R1}{R2}) \times 0.8V$$

Note that the R1 is part of the compensation. It should be conformed to the feedback compensation. If the R1 is chosen, it should not be changed to adjust output voltage; only change R2 instead. Using 1% or better resistors for the resistor divider is recommended.

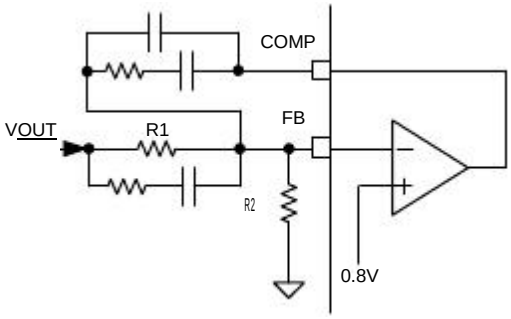


Figure 8. Resistor Divider for VDDQ and VMCH

The VTT regulator voltage is determined by REFSEN voltage, and the internal fixed resistive divider from REFSEN to the ground divides the REFSEN voltage in the ratio of 1:1. The following equation can be used to calculate the VTT output voltage:

$VTT = V_{REFSEN} \times 0.495$ - source current

$VTT = V_{REFSEN} \times 0.505$ - sink current

VTT Regulator Input/Output Capacitor Selection

The input capacitor is chosen based on its voltage rating. Under load transient condition, the input capacitor will momentarily supply the required transient current.
The output capacitor for the VTT regulator is chosen to minimize any drop during load transient condition. Higher capacitor value and lower ESR reduce the output ripple and the load transiene drop. In addition, the capacitor is chosen based on its voltage rating.
The recommended value of output capacitor is between 100∝F (min. ESR rating is 8m&) to 1000∝F (min. ESR rating is 2m&), and the maximum ESR rating is 300m&. A low-ESR aluminum electrolytic capacitor works well and provides good transient response and stability.

PWM Compensation

The output LC filter of a step down converter introduces a double pole, which contributes with –40dB/decade gain slope and 180 degrees phase shift in the control loop. A compensation network between COMP, FB, and VOUT should be added to compensate the double pole. The compensation network is shown in Figure 12.
The output LC filter consists of the output inductor and output capacitors. The transfer function of the LC filter is given by:

$$GAIN_{LC} = \frac{1+ s \cdot ESR \cdot C_{OUT}}{s^2 \cdot L \cdot C_{OUT} + s \cdot ESR \cdot C_{OUT} + 1}$$

The poles and zero of this transfer function are:

$$F_{LC} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_{OUT}}}$$

$$F_{ESR} = \frac{1}{2 \cdot \pi \cdot ESR \cdot C_{OUT}}$$

The FLC is the double poles of the LC filter, and FESR is the zero introduced by the ESR of the output capacitor.

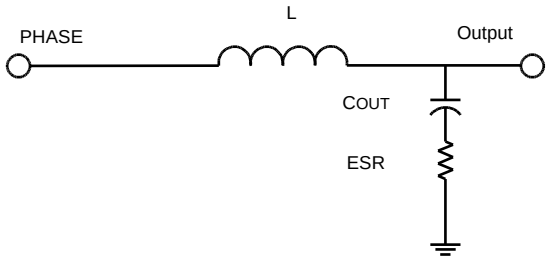


Figure 9. The Output LC Filter

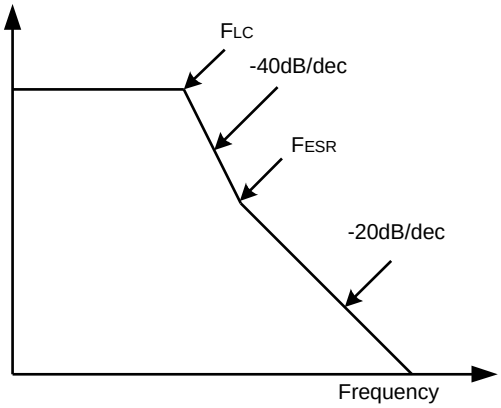


Figure 10. The LC Filter Gain & Frequency

Application Information (Cont.)

PWM Compensation (Cont.)

The PWM modulator is shown in Figure 11 The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by:

$$GAIN_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

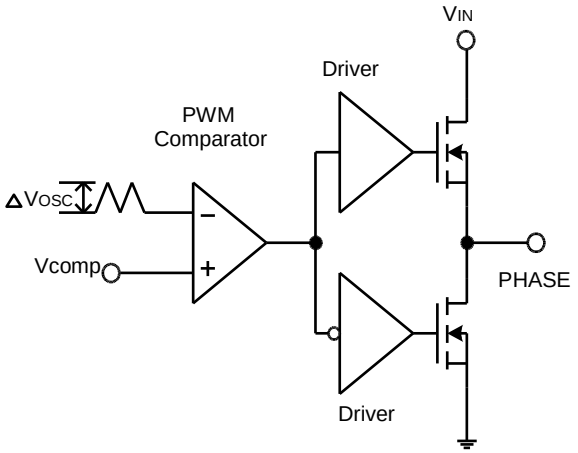


Figure 11. The PWM Modulator

The compensation circuit is shown in Figure 12. Design a appropriate compensation circuit to get the desired zero crossover frequency and sufficient phase margin. The transfer function of error amplifier is given by:

$$GAIN_{AMP} = \frac{V_{COMP}}{V_{OUT}} = \frac{\frac{1}{sC1} // \left(R2 + \frac{1}{sC2}\right)}{R1 // \left(R3 + \frac{1}{sC3}\right)}$$

$$\therefore \frac{R1+R3}{R1 \cdot R3 \cdot C1} \cdot \frac{\left(s + \frac{1}{R2 \cdot C2 \cdot (R1+R3) \cdot C3}\right)}{s\left(s + \frac{C1+C2}{R2 \cdot C1 \cdot C2}\right)\left(s + \frac{1}{R3 \cdot C3}\right)}$$

The poles and zeros of the transfer function are:

$$F_{Z1} = \frac{1}{2 \cdot \pi \cdot R2 \cdot C2}$$

$$F_{Z2} = \frac{1}{2 \cdot \pi \cdot (R1+R3) \cdot C3}$$

$$F_{P1} = \frac{1}{2 \cdot \pi \cdot R2 \cdot \left(\frac{C1 \cdot C2}{C1 + C2}\right)}$$

$$F_{P2} = \frac{1}{2 \cdot \pi \cdot R3 \cdot C3}$$

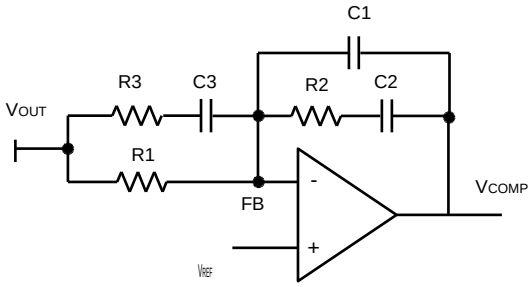


Figure 12. Compensation Network

The closed loop gain of the converter can be written as:

GAINLC x GAINPWM x GAINAMP

Figure 13 shows the asymptotic plot of the closed loop converter gain and the following guidelines will help to design the compensation network. Using the below guidelines should give a compensation similar to the curve plotted. A stable closed loop has a -20dB/decade slope and a phase margin greater than 45 degree.

1.Choose a value for R1, usually between 1K to 5K.

2.Select the desired zero crossover frequency FO:
(1/5 ~ 1/10) x FS >FO>FESR
Use the following equation to calculate R2:

$$C2 = \frac{1}{2 \cdot \pi \cdot R2 \cdot F_{LC} \cdot 0.75}$$

$$\frac{1\left(\frac{1}{sC1} \cdot \frac{1}{sC2}\right)}{}$$

$$R2 = \frac{}{} \cdot \frac{}{} \cdot R1 \qquad \left(s + \right|$$

Calculate the C1 by the equation:

$$C1 = \frac{C2}{2 \cdot \pi \cdot R2 \cdot C2 \cdot F_{ESR} \cdot \pi \cdot 1}$$

5.Set the second pole FP2 at half of the switching frequency and also set the second zero FZ2 at the output LC filter double pole FLC. The compensation gain should not exceed the error amplifier open loop gain, check the compensation gain at FP2 with the capabilities of the error amplifier.

Application Information (Cont.)

PWM Compensation (Cont.)

FP2 = 0.5xFS
FZ2 = FLC

Combine the two equations will get the following component calculations:

$$R3 = \frac{R_L}{\frac{F_S}{2xF_{LC}} - 1} \qquad C3 = \frac{1}{\pi \cdot R3 \cdot F_S}$$

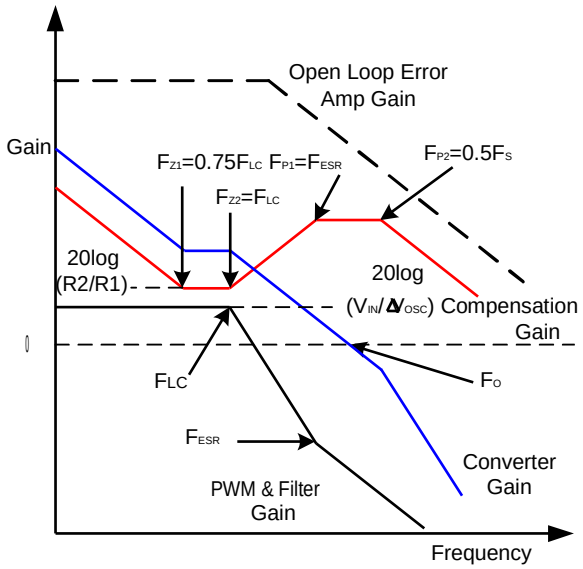


Figure 13. Converter Gain & Frequency

Output Inductor Selection

The inductor value determines the inductor ripple current and affects the load transient response. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_S \cdot L} \cdot \frac{V_{OUT}}{V_{IN}}$$

$V_{OUT} = I_{RIPPLE} \times ESR$

where F_S is the switching frequency of the regulator.

Although increases the inductor value to reduce the ripple current and voltage, there is a tradeoff existing between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current.

The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current.

Once the inductance value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is make of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

Output Capacitor Selection

Higher Capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, select high performance low ESR capacitors are intended for switching regulator applications. In some applications, multiple capacitors have to be parallelled to achieve the desired ESR value. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors also must be considered. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power-up, the input capacitors have to handle large amount of surge current. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer. For high frequency decoupling, a ceramic capacitor 1∝F can be connected between the drain of upper MOSFET and the source of lower MOSFET.

MOSFET Selection

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reverse transfer capacitance(C_{RSS}) and maximum output current requirement. The losses in the MOSFETs have two components: conduction loss and transition loss. For the upper and lower MOSFET, the losses are approximately given by the following equations:

Application Information (Cont.)

MOSFET Selection (Cont.)

$P_{UPPER} = I_{OUT\,2}(1+ TC)(R_{DS(ON)})D + (0.5)(I_{OUT})(V_{IN})(t_{SW})F_S$

$P_{LOWER} = I_{OUT\,2}(1+ TC)(R_{DS(ON)})(1-D)$

where I_{OUT} is the load current

TC is the temperature dependency of $R_{DS(ON)}$

F_S is the switching frequency

t_{SW} is the switching interval

D is the duty cycle

Note that both MOSFETs have conduction losses while the upper MOSFET includes an additional transition loss. The switching internal, t_{SW}, is the function of the reverse transfer capacitance C_{RSS}. The (1+TC) term is to factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs Temperature" curve of the power MOSFET.

Layout Consideration

In high power switching regulator, a correct layout is important to ensure proper operation of the regulator. In general, interconnecting impedances should be minimized by using short and wide printed circuit traces. Signal and power grounds are to be kept separating and finally combined to use ground plane construction or single point grounding. Figure 14 illustrates the layout, with bold lines indicating high current paths; these traces must be short and wide. Components along the bold lines should be placed close together.
Below is a checklist for your layout:

- -33The metal plate of the bottom of the packages (TSSOP-24P) must be soldered to the PCB and connect to the GND plane on the backside through several thermal vias. More vias is better for heatsink.
- -33Keep the switching nodes (UGATE, LGATE, and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible.
- Connet the FB and VTTFB to point of load and the REFSEN should be connected to the point of load of the VDDQ output.
- The traces from the gate drivers to the MOSFETs (UG1, LG1, UG2, and LG2) should be short and wide.
- Decoupling capacitor, compensation component, the resistor dividers, boot capacitors, and SS capacitors should be close to their pins.
- The input capacitor should be near the drain of the upper MOSFET; the output capacitor should be near the loads.
- The input capacitor GND should be close to the output capacitor GND and the lower MOSFET GND.
- The drain of the MOSFETs (VIN and phase nodes) should be a large plane for heat sinking.

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Application Information (Cont.)

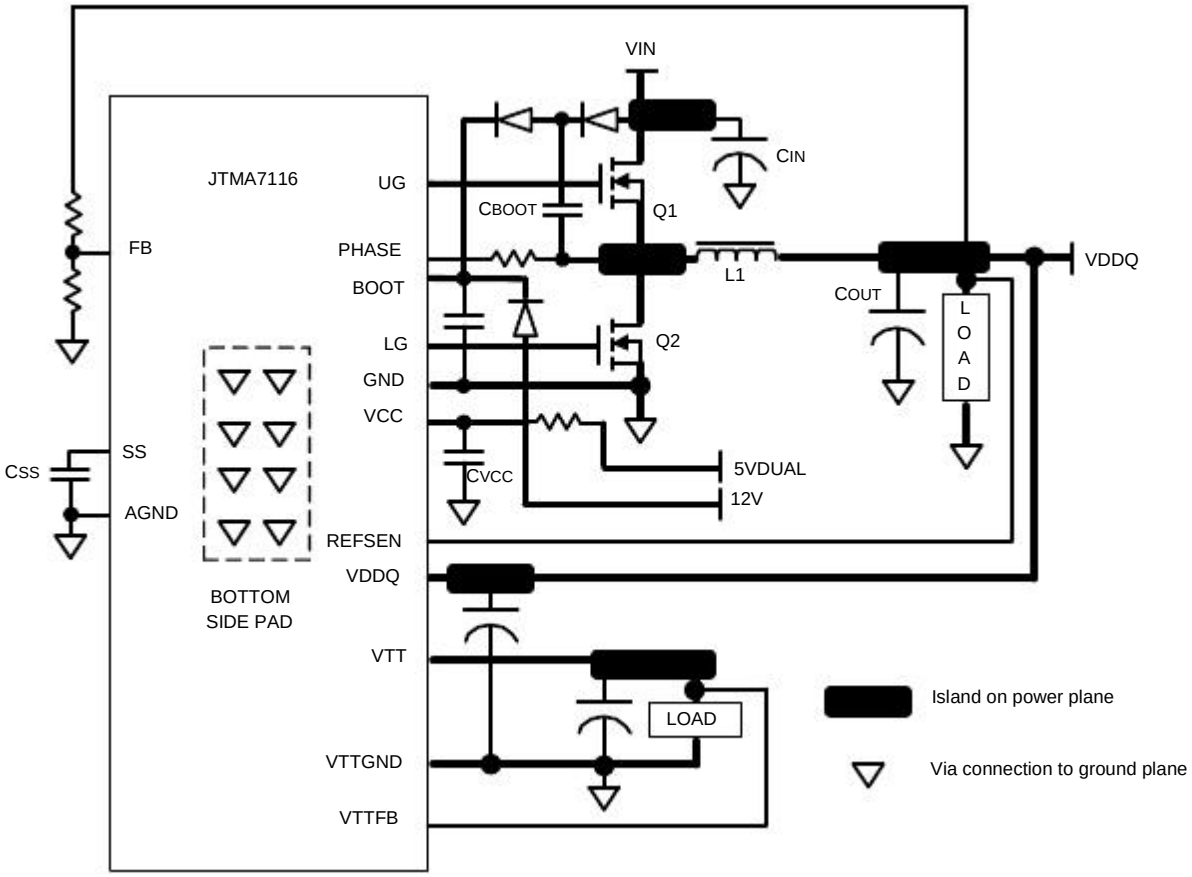
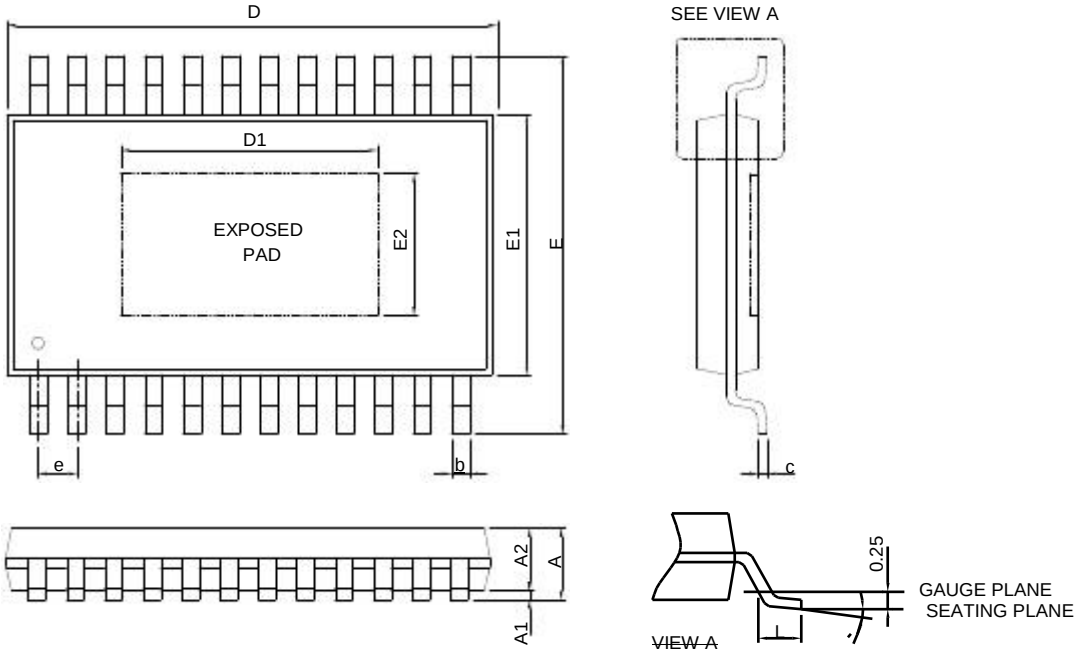


Figure 14. Layout Guidelines

Package Information

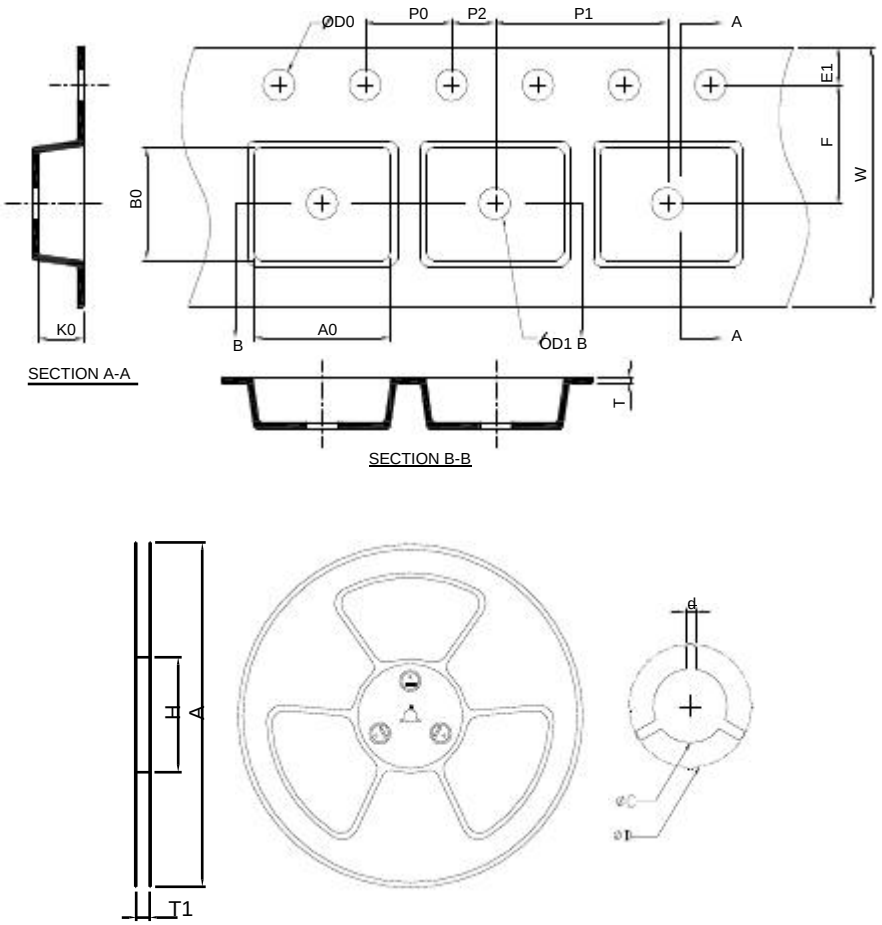
TSSOP-24P



SYMBOL	TSSOP-24P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008
D	7.70	7.90	0.303	0.311
D1	3.50	5.00	0.138	0.197
E	6.20	6.60	0.244	0.260
E1	4.30	4.50	0.169	0.177
E2	2.50	3.50	0.098	0.138
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
0	0^{o}	8^{o}	0^{o}	8^{o}

Note : 1. Followed from JEDEC MO-153 ADT.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TSSOP-24P	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.50±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.00±0.10	8.00±0.10	2.00±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.9±0.20	8.30.±0.20	1.50±0.20

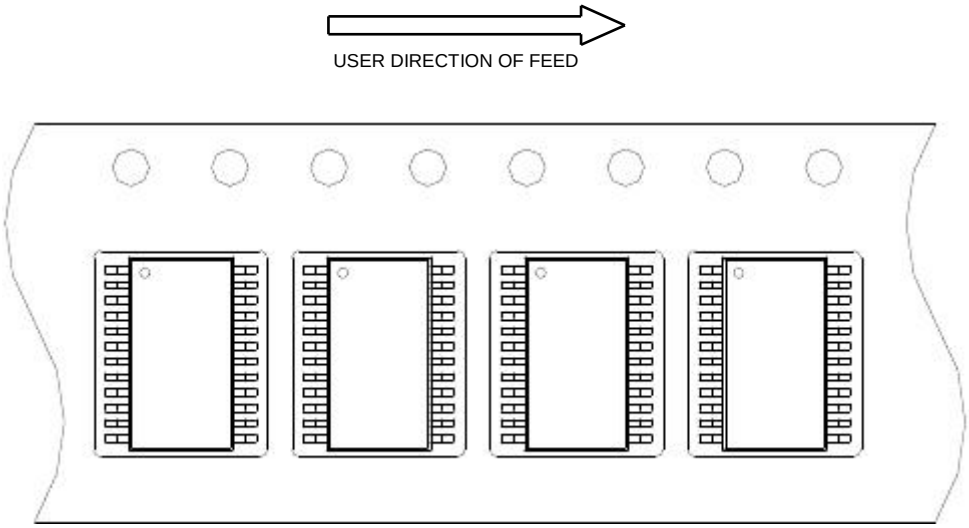
(mm)

Devices Per Unit

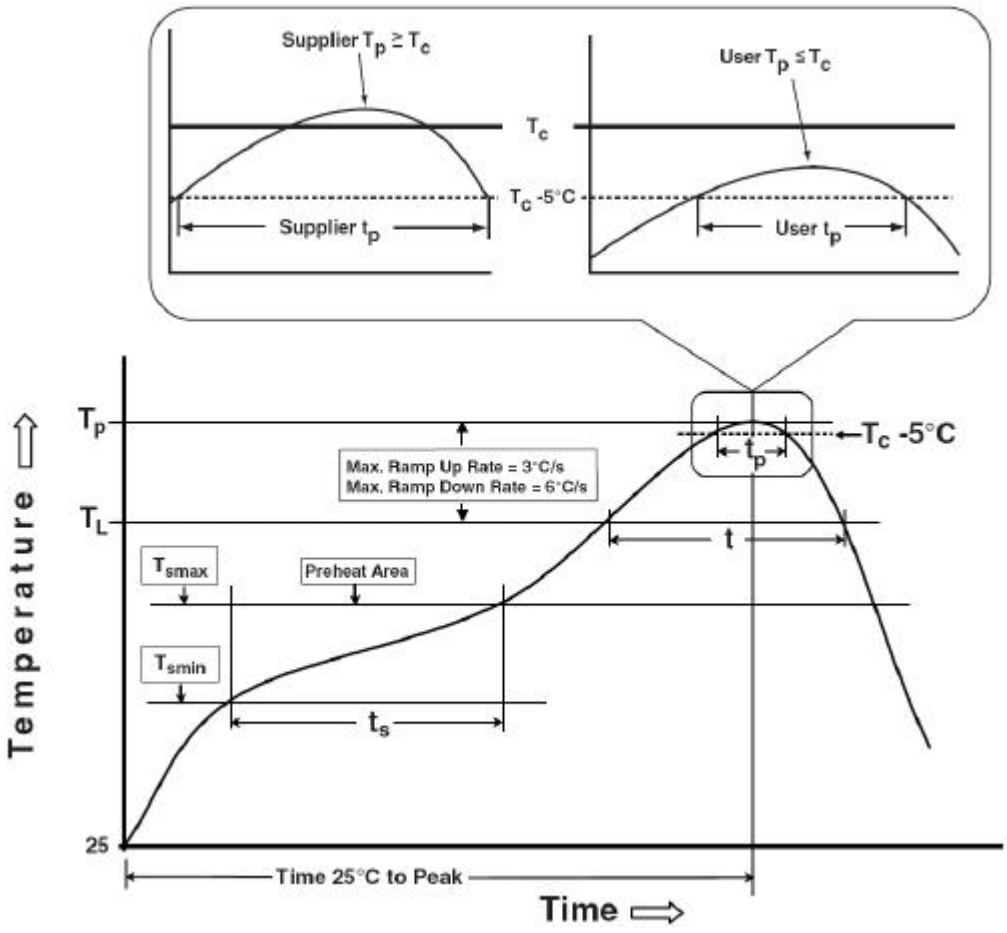
Package Type	Unit	Quantity
TSSOP-24P	Tape & Reel	2000

Taping Direction Information

TSSOP-24P



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ε350
<2.5 mm	235 °C	220 °C
ε2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
ε2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

Customer Service