Dual-Phase Synchronous-Rectifier Buck Controller

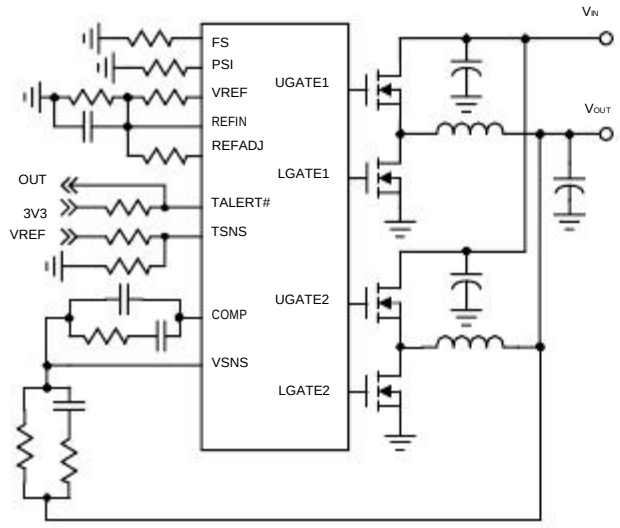
Features

- **Voltage-Mode Operation with Current Sharing**
- **Operate with 4.5V~13.2V Supply Voltage**
- **Support Single and Two-Phase Operations**
- **+/-2% Reference Voltage Accuracy Over Temperature**
- **Loss-Less Low Side MOSFET Ron Current Sensing**
- **Programmable PWM Switching Frequency from 100kHz to 800kHz**
- **Dynamic Output Voltage Adjustment**
- **TQFN4x4-24 Package**
- **Halogen and Lead Free Available (RoHS Compliant)**

General Description

The JTMA8732 is a two-phases, voltage-mode and fixed frequency buck controller.

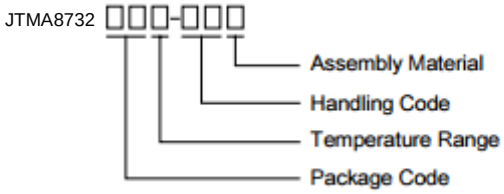
Simplified Application Circuit



Applications

- **VGA**

Ordering and Marking Information

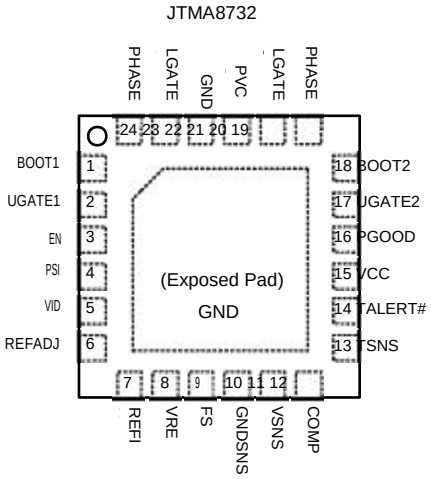


Package Code
QA: QFN4x4-24
Operating Ambient Temperature Range
I : -40 to 85 C°
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device

JTMA8732 QA: JTMA8732 XXXXX - Date Code
XXXXX

Note: JIATAIMU lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. JIATAIMU lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. JIATAIMU defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



QFN4x4-24
Top View

Absolute Maximum Ratings(Note 1)

Symbol	Parameter		Rating	Unit
V_{VCC}	Input Supply Voltage (V_{VCC} to GND)		-0.3 ~ 16	V
V_{PVCC}	Gate Driver Supply Voltage (V_{PVCC} to GND)		-0.3 ~ V_{VCC}+1	V
$V_{BOOT1/2}$	BOOT1/2 to PHASE1/2 Voltage		-0.3 ~ 16	V
	BOOT1/2 to GND Voltage		-0.3 ~ 32	V
$V_{UGATE1/2}$	UGATE1/2 to PHASE Voltage	> 200ns	-0.3 ~ $V_{BOOT1/2}$+0.3	V
		< 200ns	-5 ~ $V_{BOOT1/2}$+5	V
$V_{LAGTE1/2}$	LGATE1/2 to GND Voltage	> 200ns	-0.3 ~ V_{VCC}+0.3	V
		< 200ns	-5 ~ V_{VCC}+5	V
$V_{PHASE1/2}$	PHASE1/2 to GND Voltage	> 200ns	-0.3 ~ 16	V
		< 200ns	-5 ~ 20	V
	EN, PSI, VID, REFADJ, REFIN, VREF, FS, GNDSND, VSNS, COMP, TSNS, TALERT#, PGOOD to GND Voltage		-0.3 ~ 7	V
	FBRTN to GND		-0.3 ~ +0.3	V
P_D	Power Dissipation		2.5	W
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)		260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	TQFN4x4-24	40	°C/W
θ_{JC}	Junction-to-Case Resistance	TQFN4x4-24	15	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operation Conditions(Note 3)

Symbol	Parameter	Range	Unit
V_{VCC}	VCC Supply Voltage (V_{VCC} to GND)	4.5 ~ 13.2	V
V_{OUT}	VOUT to GND	0.6 ~ 5.5	V
V_{IN}	Converter Input Voltage	2.9 ~ V_{VCC}+1	V
F_{OSC}	Oscillator Frequency	100 ~ 800	kHz
I_{OUT}	Converter Output Current	0 ~ 60	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit

Electrical Characteristics

(Refer to figure 1 in the "Typical Application Circuits". These specifications apply over V_{VCC} = 12V, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C.)

Symbol	Parameter	Test Conditions	JTMA8732			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
VCC	Supply Voltage Range		4.5	-	13.2	V
I_{VCC_SD}	Input DC Bias Current	No switching, EN=GND	-	-	300	uA
I_{VCC}		UGATE1/2, LGATE1/2 open, switching	-	-	10	mA
I_{PVCC_SD}	Input DC Bias Current	No switching, EN=GND	-	-	100	uA
I_{PVCC}		UGATE1/2, LGATE1/2 open, switching	-	-	100	uA
	POR Threshold of VCC		4.1	4.3	4.5	V
	POR Hysteresis		-	0.2	-	V
	POR Threshold of PVCC		4.1	4.3	4.5	V
	POR Hysteresis		-	0.2	-	V
CHIP ENABLE/FREQUENCY SETTING						
I_{FS}	FS Source Current	FS=GND	100	150	200	uA
V_{FS}	FS Voltage	R_{FS}=33kΩ	-	1	-	V
	Switching Frequency Setting Range		100	-	800	kHz
F_{OSC}	Free Run Switching Frequency	R_{FS}=33kΩ	270	300	330	kHz
ΔF_{OSC}	Switching Frequency Accuracy	F_{OSC}=200kHz~500kHz	-15	-	15	%
CHIP ENABLE						
	Chip Enable Threshold		1.6	-	-	V
	Chip Shutdown Threshold		-	-	0.8	V
OSCILLATOR						
	Maximum Duty Cycle		70	80	90	%
	Minimum Duty Cycle		-	0	-	%
ΔV_{OSC}	Ramp Amplitude	V_{VCC}=12V, RAMP peak to peak = 1~3V	-	2	-	V
POWER GOOD INDICATOR						
	PGOOD Pull Low Resistance	I_{PGOOD}=100mA	-	-	50	Ω
	PGOOD High Threshold	V_{SNS} Rising	115	120	125	$\%V_{REFIN}$
	Hysteresis		-	5	-	$\%V_{REFIN}$
	PGOOD Low Threshold	V_{SNS} Falling	75	80	85	$\%V_{REFIN}$
	Hysteresis		-	5	-	$\%V_{REFIN}$
POWER SAVING MODE						
V_{PSI}	Threshold Voltage to Enter Dual Phase	V_{PSI} Rising	1.9	2.0	2.1	V
	Hysteresis Voltage to Enter Dual Phase	V_{PSI} Falling.	-	0.3	-	V
V_{PSI}	Threshold Voltage to Enter DCM	V_{PSI} Falling	0.9	1	1.1	V
	Hysteresis Voltage to Enter DCM	V_{PSI} Rising	-	0.3	-	V
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage Accuracy	I_{REF}=100uA, **T_J= -20 C ~ 70 C**	1.98	2.00	2.02	V
	VREF Maximum Output Current	VREF=GND	-	10	-	mA
ΔV_{REF}	Reference Voltage Load Regulation	I_{REF}=0~2mA	-5	-	5	mV
	Output Voltage Accuracy	V_{REFIN}-V_{VSNS}, V_{REFIN}=0.2V~2V, V_{GNDSNS}=GND	-5	-	5	mV
	V_{REFIN} Operating Range		0.2	-	2	V
	REFIN Input Leakage Current		-	-	0.1	uA

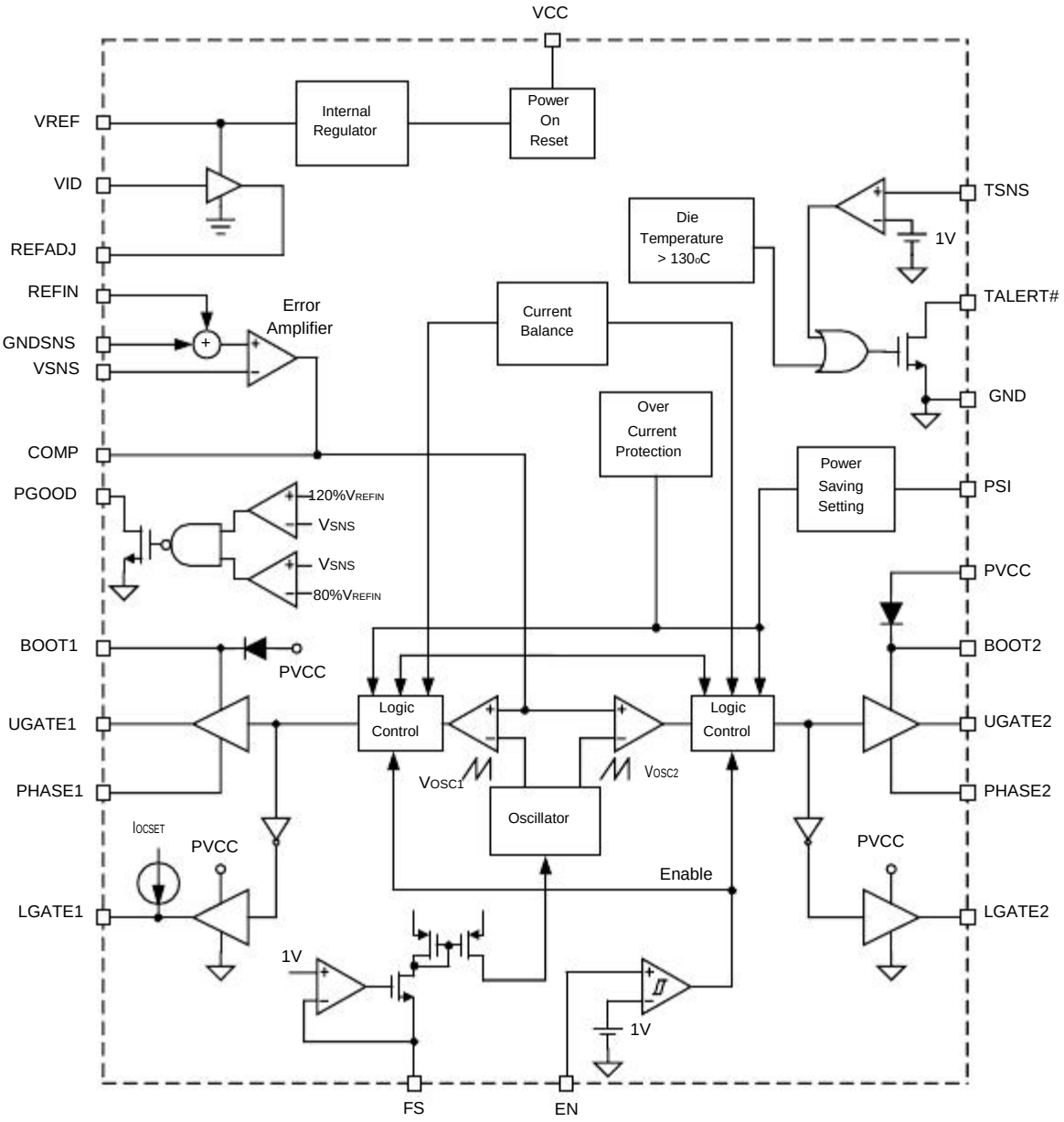
ERROR AMPLIFIER						
	Open-Loop DC Gain (Note 4)	R_L = 10k∧, C_L =10pF	70	80	-	V/V
	Open-Loop Bandwidth (Note 4)	R_L = 10k∧, C_L =10pF	15	20	-	MHz
	Slew Rate (Note 4)	R_L = 10k∧, C_L =10pF	-	8	-	V/us
	FB Input Leakage Current	V_{FB}=1.6V	-	0.1	0.5	uA
V_{COMP}	COMP High Voltage	R_L = 10k∧, C_L =10pF	-	4.8	-	V
	COMP Low Voltage	R_L = 10k∧, C_L =10pF	-	0.2	-	V
I_{COMP}	Maximum COMP Source Current	V_{COMP}=2V	-	2	-	mA
	Maximum COMP Sink Current	V_{COMP}=2V	-	2	-	mA
VID CONTROL INPUT						
V_{IH}	Logic High Threshold Level		2.5	-	-	V
V_{IL}	Logic Low Threshold Level		-	-	0.8	V
	Output High Impedance	Tri-state	0.8	-	2.5	V
	VID Input Leakage Current	VID=3.3V	-	-	1	uA
REFADJ DRIVING						
T_R	REFADJ Rising Time	With 20pF Load	-	5	10	ns
T_F	REFADJ Falling Time	With 20pF Load	-	5	10	ns
	Rising and Falling Edge Delay	$\|T_R-T_F\|$	-	-	0.5	ns
T_{PDR}	Rising Propagation Delay	50%VID to 50%V_{REFADJ} with 20pF Load	-	10	-	ns
T_{PDF}	Falling Propagation Delay	50%VID to 50%V_{REFADJ} with 20pF Load	-	10	-	ns
ΔT_{PD}	Propagation Delay Error	$\|T_{PDR}-T_{PDF}\|$	-	-	0.5	ns
T_U	Unit Pulse Width		-	27	-	ns
ZERO CURRENT DETECT						
V_{ZC}	Zero Current Detect	V_{PHASE1}-GND	-3	-	3	mV
Gate Driver						
R_{UG_SRC}	Upper Side Gate Sourcing	I_{UGATE}=100mA Sourcing	-	2	4	Ω
R_{UG_SNK}	Upper Side Gate Sinking	I_{UGATE}=100mA Sinking	-	1.5	3	Ω
R_{LG_SRC}	Low Side Gate Sourcing	I_{LGATE}=100mA Sourcing	-	2	4	Ω
R_{LG_SNK}	Low Side Gate Sinking	I_{LGATE}=100mA Sinking	-	1	2	Ω
T_{DT}	Dead-time		-	20	-	ns
PROTECTION						
	Under Voltage Protection (UVP)	$V_{SNS-GND}/V_{REFIN-GND}$	40	45	50	%
	UVP Debounce time		-	2	-	us
I_{OCSET}	OCP Setting Current		9	10	11	uA
	OCP Delay Time		-	2	-	us
	OCP DAC Sample Delay Time		-	64	-	clock
	OCP DAC Sample Time		-	127	-	clock
	Over Temperature Protection (OTP)		-	150	-	°C
	Over Temperature Hysteresis		-	30	-	°C
	Maximum V_{OCSET} Threshold		0.55	0.6	-	V
$T_{ALERT\#}$	Thermal Alert		-	130	-	°C
V_{TSNS}	Temperature Sense Threshold		0.95	1	1.05	V
	Temperature Sense Hysteresis		-	0.1	-	V
	Thermal Alert Pull Low Resistance	$I_{TALERT\#}$=100mA	-	-	50	Ω

Note 4: Guarantee by design, not production test

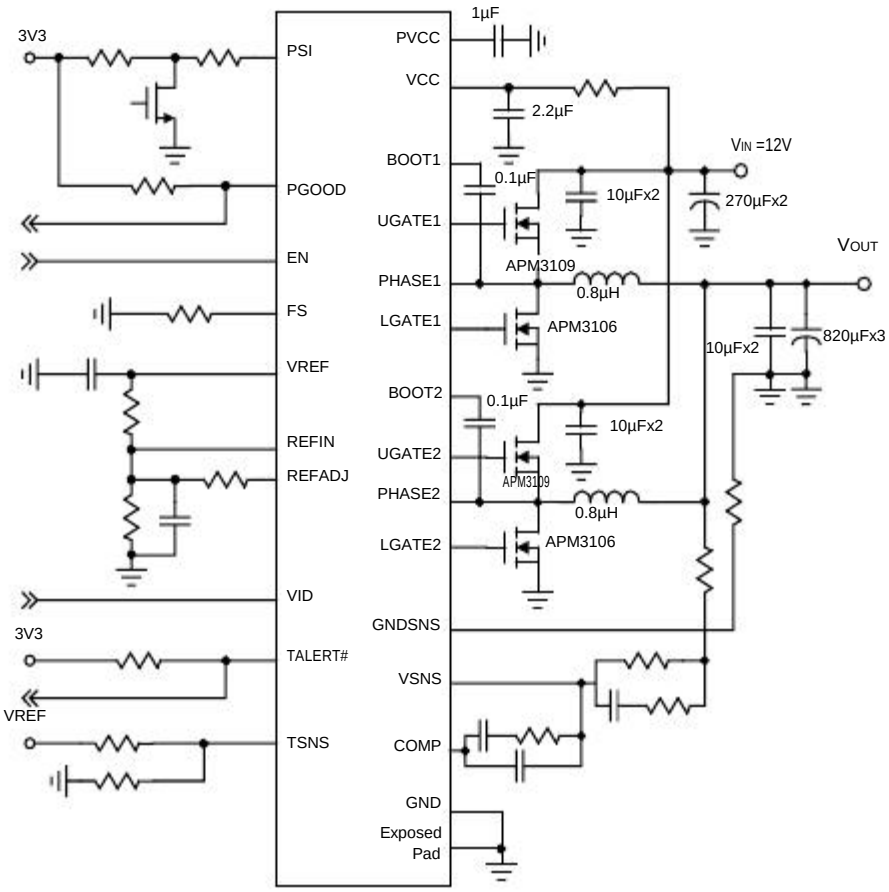
Pin Descriptions

PIN	NAME	FUNCTION
1	BOOT1	Bootstrap Supply for the floating high-side gate driver of channel 1. Connect the Bootstrap capacitor between the BOOT1 pin and the PHASE1 pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the high-side MOSFET. Typical values for CBOOT range from 0.1μF to 1μF.Ensure that CBOOT is placed near the IC.
2	UGATE1	Upper Gate Driver Output for channel 1. Connect this pin to the gate of high-side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET has turned off.
3	EN	Enable input.
4	PSI	**Power Saving Mode.** Connect a resistor from PSI to GND to set the power saving mode threshold current level. Connect this pin to VREF for always two phases operation. Short this pin to ground for always single-phase operation.
5	VID	**VID Input.** This pin is used to adjust reference voltage.
6	REFADJ	Reference adjustment output.
7	REFIN	**External Reference Input.** This is input pin of external reference voltage. Connect a voltage divider from VREF to REFIN to FBRTN to set the reference voltage.
8	VREF	**Reference Voltage Output.** This is the output pin of high precision 2V reference voltage. Bypass this pin with a 1uF ceramic capacitor to FBRTN.
9	FS	**Operation Frequency Setting.** Connecting a resistor between this pin and GND to set the operation frequency.
10	GNDSNS	**GND Sense.** Negative node of the remote voltage sense.
11	VSNS	**Feedback Voltage.** This pin is the inverting input to the error amplifier. Use this pin in combination with the COMP pin to compensate the voltage control feedback loop of the converter.
12	COMP	**Error Amplifier Output.** This is the output of the error amplifier (EA) and the non-inverting input of the PWM comparators. Use this pin in combination with the FB pin to compensate the voltage-control feedback loop of the converter.
13	TSNS	**Temperature sensing input.**
14	TALERT#	**Thermal Alert.** Active low open drain output.
15	VCC	**Supply Voltage.** This pin provides current for internal control circuit and PVCC. Bypass this pin with a minimum 1uF ceramic capacitor next to the IC.
16	PGOOD	Open drain power good output.
17	UGATE2	Upper Gate Driver Output for channel 2. Connect this pin to the gate of high-side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET has turned off.
18	BOOT2	Bootstrap Supply for the floating high-side gate driver of channel 2. Connect the Bootstrap capacitor between the BOOT2 pin and the PHASE2 pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the high-side MOSFET. Typical values for CBOOT range from 0.1μF to 1μF.Ensure that CBOOT is placed near the IC.
19	PHASE2	Switch Node for Channel 2. Connect this pin to the source of high-side MOSFET and the drain of the low-side MOSFET. This pin is used as sink for UGATE2 driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET has turned off.
20	LGATE2	Low-side Gate Driver Output for Channel 2. Connect this pin to the gate of low-side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the low-side MOSFET has turned off.
21	PVCC	**Supply Voltage for Gate Driver.** This pin is the output of internal 9V LDO. This pin provides current for gate drives. Bypass this pin with a minimum 1uF ceramic capacitor.
22	GND	Ground.
23	LGATE1	Low-side Gate Driver Output for Channel 1. Connect this pin to the gate of low-side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the low-side MOSFET has turned off.
24	PHASE1	Switch Node for Channel 1. Connect this pin to the source of high-side MOSFET and the drain of the low-side MOSFET. This pin is used as sink for UGATE1 driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET has turned off.
Exposed Pad	PGND	**Power Ground.** Tie this pin to the ground island/plane through the lowest impedance connection available.

Block Diagram



Typical Application Circuit



Function Descriptions

VCC Power-On-Reset (POR)

The Power-On-Reset (POR) circuit compares the input voltage at VCC with the POR threshold (4.3V rising, typical) to ensure the input voltage is high enough for reliable operation. The 0.2V (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the POR rising threshold, startup begins. When the input voltage falls below the POR falling threshold, the controller turns off the converter.

PVCC Power-On-Reset (POR)

The Power-On-Reset (POR) circuit compares the input voltage at PVCC with the POR threshold (4.3V rising, typical) to ensure the input voltage is high enough for reliable operation. The 0.2V (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the POR rising threshold, startup begins. When the input voltage falls below the POR falling threshold, the controller turns off the converter.

VREF

This is the output pin of high precision 2V reference voltage. Bypass this pin with a 1uF ceramic capacitor to GND. The VREF must have capability to drive 10mA output current.

Soft-start

After the VCC/PVCC voltage exceeds the POR voltage threshold and the EN threshold exceeds 1V, the device initials a start-up process and then ramps up the output voltage to the setting of output voltage. A 10mA current source starts to charge the capacitor (C_{VREF}) connected with VREF and GND pins. The REFIN voltage is divided by the resistor R_{VREF1} and R_{VREF2}. The V_{REFIN} starts to rise with the same rise rate as the VREF voltage. When the VREF voltage reaches 90%, the soft-start process is completed.

$T_{SS}=C_{VREF}*2V/10mA$

Since the VREFIN soft-start, to prevent PGOOD abnormal trigger during soft-start. The PGOOD enabled after VREF>1.8V.

VID adjust from VBOOT to VOUT should be normal (BW is large enough).

FS

Connecting a resistor between FS and GND to set the operation frequency.

FS(kohm) x Fosc (kHz) = 10000 (MΩHz)

FS(kohm)	Fosc
10k	1000kHz
50k	200kHz
100k	100kHz
200k	50kHz

Current Sense

The JTMA8732 sense low side MOSFET

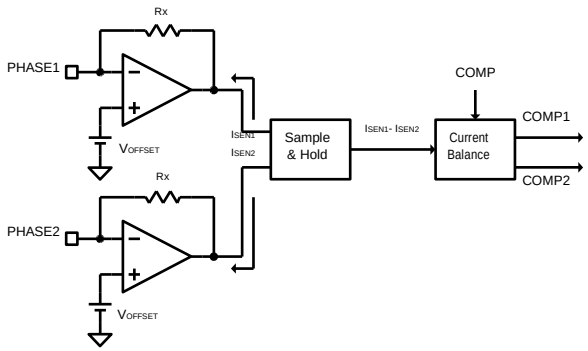
Current Sharing

The JTMA8732 extracts phase currents for current balance by parasitic on-resistance of the lower switches when turned on as shown in Figure 5. The GM amplifier senses the voltage drop across the lower switch and converts it into current signal each time it turns on. The sampled and held current is expressed as:

$I_{SENx} = Gm \times \Delta V = (PGND-VSW)/RX + V_{OFFSET}/RX$

$= I_{LX} \times R_{DS(ON)}/RX + V_{OFFSET}/RX$

The differential current of the current sharing control circuit (I_{SEN1}-I_{SEN2}) is used to generate two current parts, I_1 and I_2. The V_{COMP1} and V_{COMP2} will increase or decrease because of these two currents. For example, when $I_{SEN1}>I_{SEN2}$, the V_{COMP1} will decrease and the V_{COMP2} will increase. Therefore, the duty of PWM1 will decrease and the duty of PWM2 will increase. Then, the device will reduce I_{L1} current and increase I_{L2} current for current sharing, vice verse.



Automatic Phase Reduction (PSI)

The JTMA8732 features automatic phase reduction that turns off phase 2 at light load condition and reduces both switching and conduction losses. The automatic phase reduction maintains high power conversion efficiency over the output current range. The output current is sensed and mirrored to PSI pin as:

V_{PSI}= (IL1*RLG1+IL2*RLG2)/800*R_{PSI}

V_{PSI}~=I_{OUT}*Ron/800*R_{PSI}

The JTMA8732 operates in dual phase if VPSI is higher than 2.0V and in single phase DCM if V_{PSI} is lower than 1V.

VPSI Level		Phase Configuration	Debounce Time (us)
>2.0V	V_{PSI} Rising	Dual Phase	No
<1.7V	V_{PSI} Falling	Single Phase PWM	240us

<1V	V_{PSI} Falling	Single Phase DCM	240us
>1.3V	V_{PSI} Rising	Single Phase PWM	No

Over Current Protection (OCP)

I_{OCSET}*R_{OCSET}=(IL1*RLG1+IL2*RLG2)~=I_{OUT}*Ron

Over-Temperature Protection (OTP)

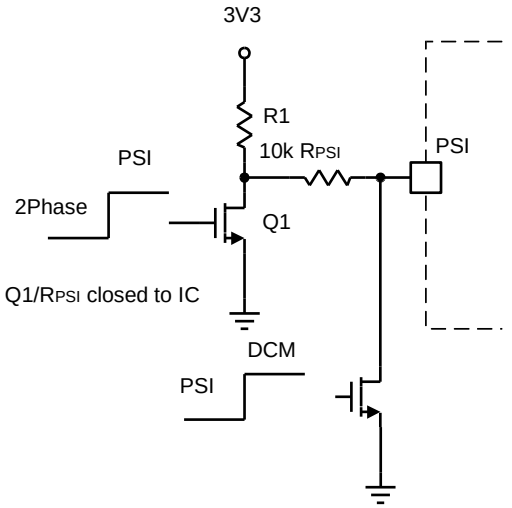
The over-temperature circuit limits the junction temperature of the JTMA8732. When the junction temperature exceeds 150 C°, a thermal sensor pulls UGTAE and LGATE low, allowing the devices to cool. The thermal sensor allows the converters to start a soft-start process and regulate the output voltage again after the junction temperature cools by 30 C.° The OTP is designed with a 40 C° hysteresis to lower the average Junction Temperature (T_J) during continuous thermal overload conditions, increasing the lifetime of the device.

OVP

The over-voltage protection (OVP) circuit monitors the FB (V_{FB}) voltage to prevent the output from over-voltage. When the V_{FB} rises to 150% of the EAP voltage (V_{EAP}), the JTMA8732 turns off high-side and turn on low-side MOSFETs to sink output voltage (V_{OUT}). As soon as the V_{FB} falls below 125% of V_{EAP}, the OVP comparator is disengaged. The chip will restore its normal operation.

UVP

The under-voltage protection circuit monitors the voltage on FB (V_{FB}) by Under-Voltage (UV) comparator to protect the PWM converter against short-circuit conditions. When the V_{FB} falls below the falling UVP threshold (50% V_{EAP}), a fault signal is generated and the device turns off high-side and low-side MOSFETs. The converter shuts down and the output is latched to be floating.



VID

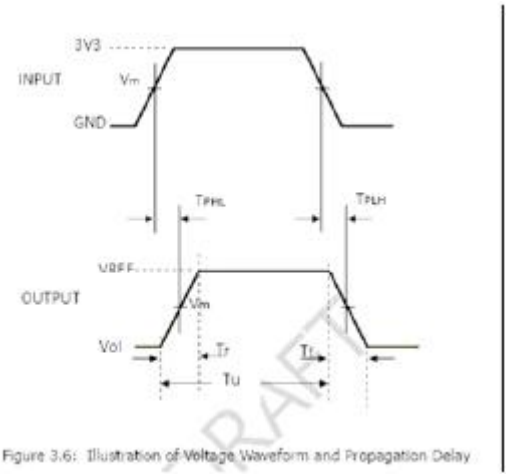


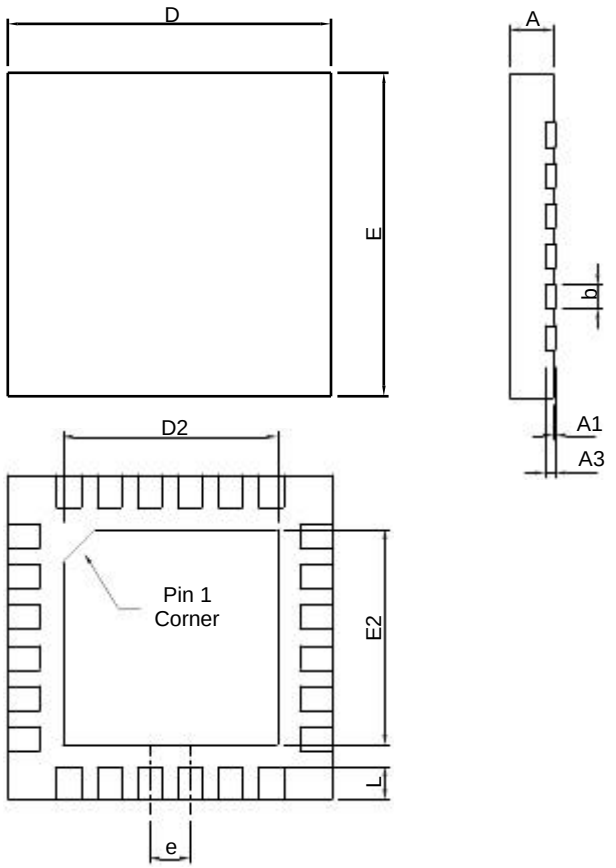
Figure 3.6: Illustration of Voltage Waveform and Propagation Delay

Table 3.2: Buffer Electrical Characteristics

Parameter	Sym	Min	Typ	Max	Units	Notes
Buffer Supply Voltage			VREF		V	
Unit Pulse Width	Tu		27		ns	Configurable
Buffer Output Rise Time	Tr		5		ns	
Buffer Output Fall Time	Tf		5		ns	
Rising and Falling Edge Delay	ΔT			0.5	ns	ΔT = | Tf - Tl |
Propagation Delay	Tpd		10		ns	Tpd = TPHL =TPLH
Propagation Delay Error	ΔTpd			0.5	ns	ΔTpd = TPHL - TPLHH

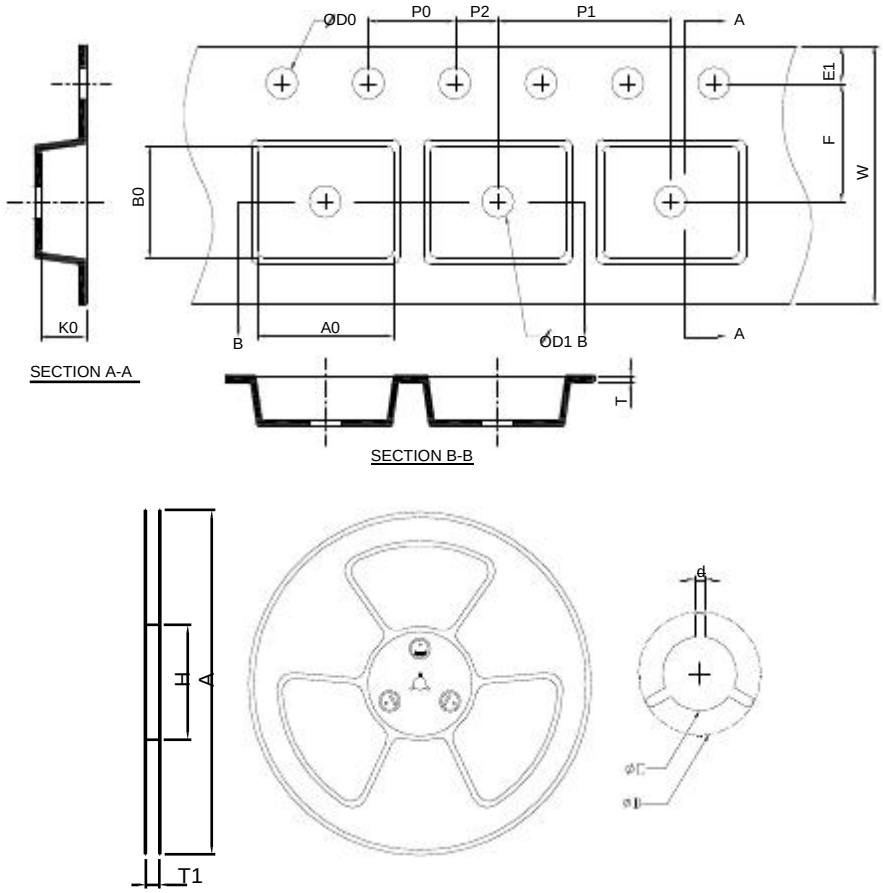
Package Information

QFN4x4-24



SYMBOL	QFN4x4-24			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.008	0.012
D	4.00 BSC		0.157 BSC	
D2	2.50	2.80	0.098	0.110
E	4.00 BSC		0.157 BSC	
E2	2.50	2.80	0.098	0.110
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
QFN4x4-24	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.30±0.20

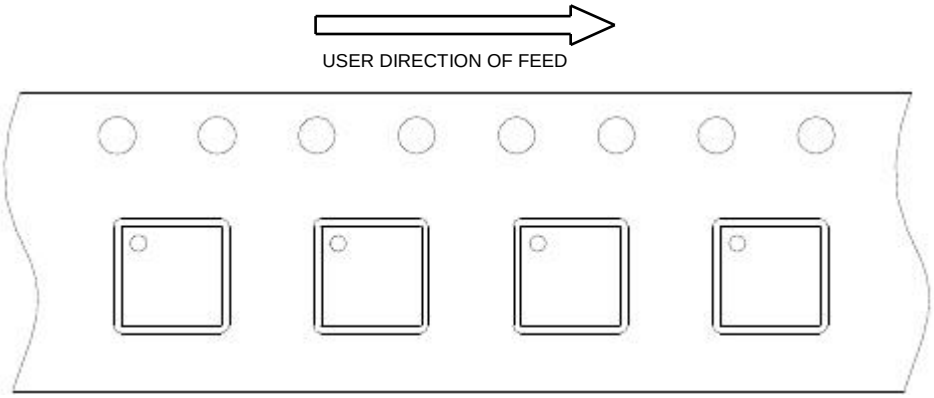
(mm)

Devices Per Unit

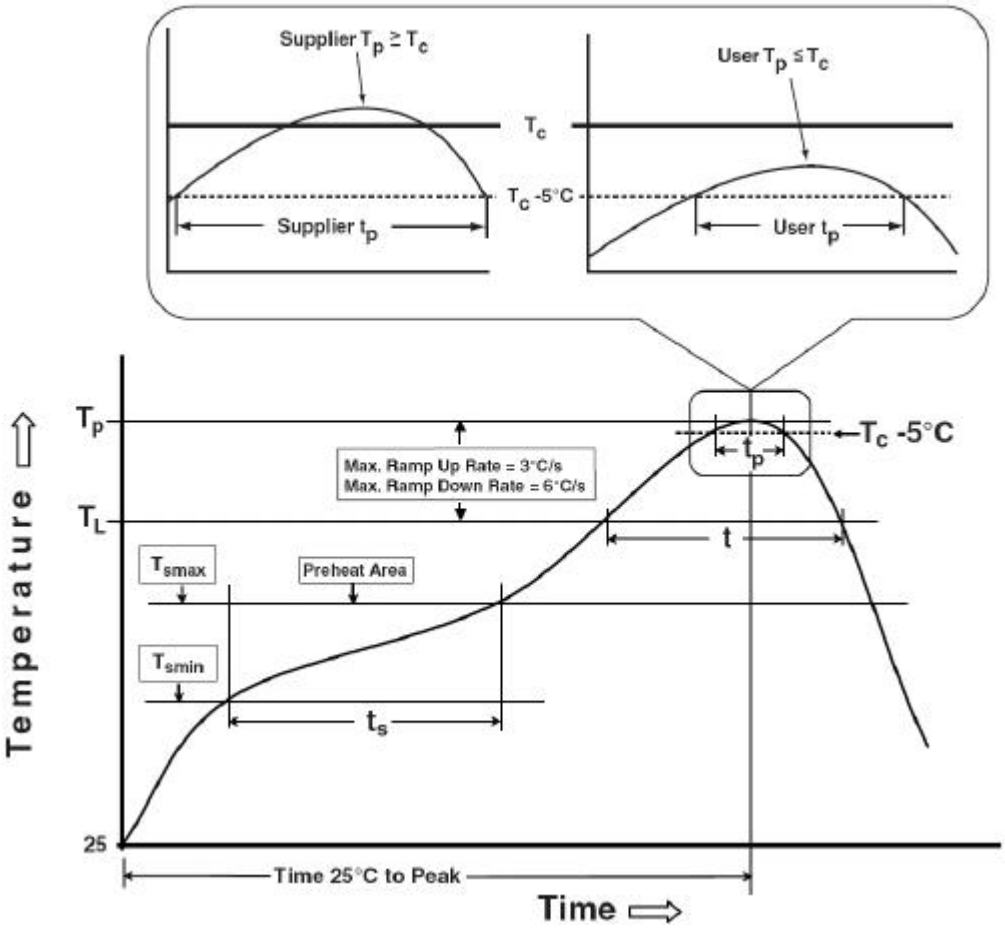
Package Type	Unit	Quantity
QFN4x4-24	Tape & Reel	3000

Taping Direction Information

QFN4x4-24



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ε350
<2.5 mm	235 °C	220 °C
ε2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
ε2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

Customer Service