

# JTMA7176

## Dual 1.5MHz, 1A Synchronous Step-Down Converter

### Features

- 1A Output Current on Each Channel
- 2.7V to 5.5V Input Voltage Range
- 1.5MHz Constant Frequency Operation
- Low Dropout Operation at 100% Duty Cycle
- Synchronous Topology
- 0.6V Low Reference Voltage
- Current Mode Operation
- Over-Temperature Protection
- Over-Current Protection
- Up to 94% Efficiency
- Internally Compensated
- Lead Free and Green Devices Available (RoHS Compliant)

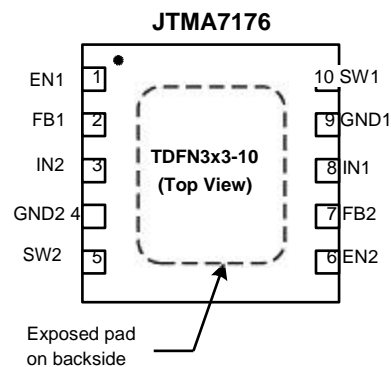
### Applications

- TV Tuner/Box
- Portable Instrument

### General Description

The JTMA7176 consists of two independent 1.5MHz constant frequency, current mode, and PWM step-down converters. Each converter integrates a main switch with a synchronous rectifier for high efficiency without an external Schottky diode. The JTMA7176 is ideal for powering portable equipment that runs from a single cell Lithium-Ion (Li+) battery. Each converter can supply 1A of load current from a 2.7V to 5.5V input voltage. The output voltage can be regulated as low as 0.6V. The JTMA7176 can also run at 100% duty cycle for low dropout applications.

### Pin Configuration



### Ordering and Marking Information

<p>JTMA7176    □□□-□□□</p> <p>Assembly Material</p> <p>Handling Code</p> <p>Temperature Range</p> <p>Package Code</p>		<p>Package Code</p> <p>QB : TDFN3x3-10</p> <p>Temperature Range</p> <p>I : -40 to 85 C°</p> <p>Handling Code</p> <p>TR : Tape &amp; Reel</p> <p>Assembly Material</p> <p>G : Halogen and Lead Free Device</p>
JTMA7176 QB:	JTMA 7176 XXXXX	XXXXX - Date Code

Note: JIATAIMU lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. JIATAIMU lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. JIATAIMU defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

JIATAIMU reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

# JTMA7176

## Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
$V_{IN1/IN2}$	Input Supply Voltage (IN1/IN2 to GND1/GND2)	-0.3 ~ 6	V
$V_{FB1/FB2}$	Voltage on FB1 and FB2 (FB1/FB2 to GND1/GND2)	-0.3 ~ $V_{IN1/IN2}+0.3$	V
$V_{EN1/EN2}$	Voltage on EN1 and EN2 (EN1/EN2 to GND1/GND2)	-0.3 ~ $V_{IN1/IN2}+0.3$	V
$V_{SW1/SW2}$	Voltage on SW1 and SW2 (SW1/SW2 to GND1/GND2)	-0.3 ~ $V_{IN1/IN2}+0.3$	V
$I_{SW\_PEAK}$	Peak SW Current	1.8	A
$P_D$	Maximum Power Dissipation ( $T_A=25^{\circ}\text{C}$ )	2	W
$T_J$	Maximum Junction Temperature	150	$^{\circ}\text{C}$
$T_{STG}$	Storage Temperature Range	-65 ~ 150	$^{\circ}\text{C}$
$T_{SDR}$	Maximum Lead Soldering Temperature, 10 Seconds	260	$^{\circ}\text{C}$

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
$\theta_{JA}$	Junction-to-Ambient Resistance in Free Air <sup>(Note 2)</sup> TDFN3x3-10	50	$^{\circ}\text{C/W}$
$\theta_{JC}$	Junction-to-Case Resistance in Free Air TDFN3x3-10	12	

Note 2:  $\theta_{JA}$  is measured on with the device mounted the PCB with top-layer pad of approximate 1" square of 1 oz copper.

## Recommended Operating Conditions

Symbol	Parameter	Range	Unit
$V_{IN1/IN2}$	Input Supply Voltage (IN1/IN2 to GND1/GND2)	2.7 ~ 5.5	V
$R2/R4$	Feedback Resistance <sup>(Note 3)</sup>	~ 300	k $\Omega$
$I_{OUT}$	Output Current	0 ~ 1	A
$T_A$	Operating Ambient Temperature	-40 ~ 85	$^{\circ}\text{C}$
$T_J$	Operating Junction Temperature	-40 ~ 125	$^{\circ}\text{C}$

Note 3: Please refer to the typical application circuit.

## Electrical Characteristics

The denotes the specifications that apply over  $V_{IN}=3.6\text{V}$  and  $T_A=25^{\circ}\text{C}$ , unless otherwise specifications.

Symbol	Parameter	Test Conditions	APW7176			Unit
			Min.	Typ.	Max.	
$V_{IN1/IN2}$	Each Converter Input Voltage Range		2.7	-	5.5	V
$I_{FB1/FB2}$	FB1/FB2 Input Current	$V_{FB1/FB2}=0.6\text{V}$	-30	-	30	nA
$V_{REF1/REF2}$	Each Converter Reference Voltage	$I_{OUT}=0\text{mA}\sim 1\text{A}$	0.588	0.6	0.612	V
$\square V_{REF1/REF2}$	Each Converter Reference Voltage Line Regulation	$-40^{\circ}\text{C}\delta T_A\delta 85^{\circ}\text{C}$	-	0.04	-	%/V
$I_{PK}$	Each Converter Peak Inductor Current	$V_{IN1/IN2}=3.3\text{V}$ , $V_{FB}=0.5\text{V}$ or $V_{OUT}=90\%$ , Duty cycle < 35%	1.4	1.6	-	A

## Electrical Characteristics (Cont.)

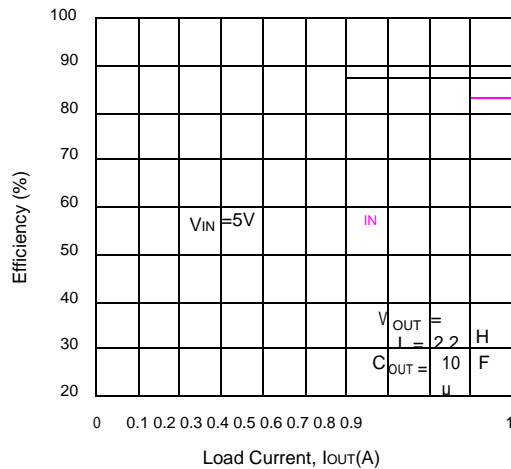
The denotes the specifications that apply over  $V_{IN}=3.6V$  and  $T_A=25^{\circ}C$ , unless otherwise specifications.

Symbol	Parameter	Test Conditions	APW7176			Unit
			Min.	Typ.	Max.	
	Each Converter Load Regulation	$I_{OUT}=10mA\sim 1A$	-	0.5	-	%
$I_{DD}$	Each Converter Quiescent Current	$V_{FB}=0.7V$	-	30	50	$\mu A$
$I_{SD}$	Each Converter Quiescent Current in Shutdown	$V_{EN1/EN2}=0V, V_{IN}=4.2V$	-	-	1	$\mu A$
$f_{OSC}$	Each Converter Oscillator Frequency	$V_{FB}=0.6V$	1.2	1.5	1.8	MHz
$f_{OSC\_FFB}$	Each Converter Frequency Foldback	$V_{FB}=0V$	-	210	-	kHz
$R_{DS-P}$	Each Converter On Resistance of PMOSFET	$I_{SW}=100mA$	-	0.28	-	$\Omega$
$R_{DS-N}$	Each Converter On Resistance of NMOSFET	$I_{SW}=-100mA$	-	0.25	-	$\Omega$
$V_{EN1/EN2}$	Each Converter Enable Threshold		0.4	-	1	V
$T_{OTP}$	Thermal Shutdown Threshold		-	150	-	$^{\circ}C$
	Thermal Shutdown Hysteresis		-	50	-	$^{\circ}C$

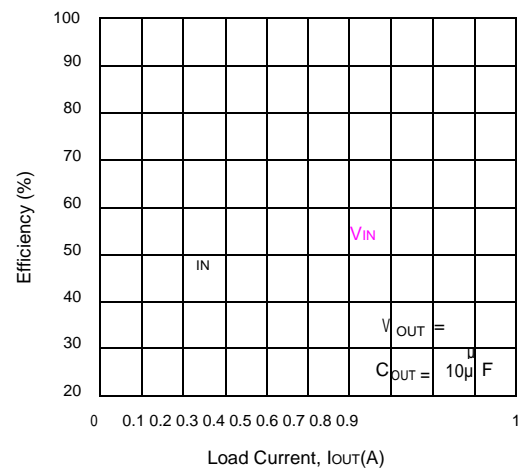
## Typical Operating Characteristics

(Refer to the application circuit in the section “Typical Application Circuits”,  $V_{IN}=3.6V$ ,  $V_{OUT}=1.8V$ ,  $T_A=25^{\circ}C$  unless otherwise specified )

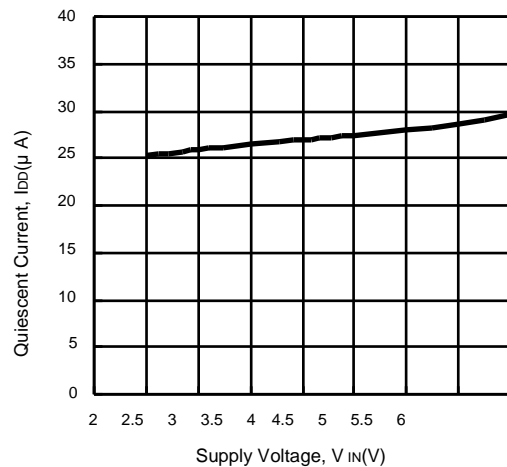
Efficiency vs. Load Current



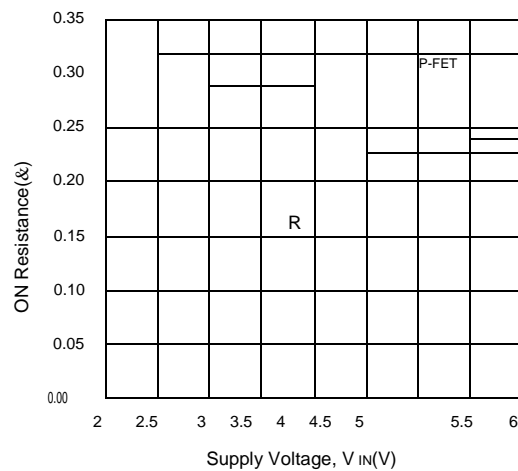
Efficiency vs. Load Current



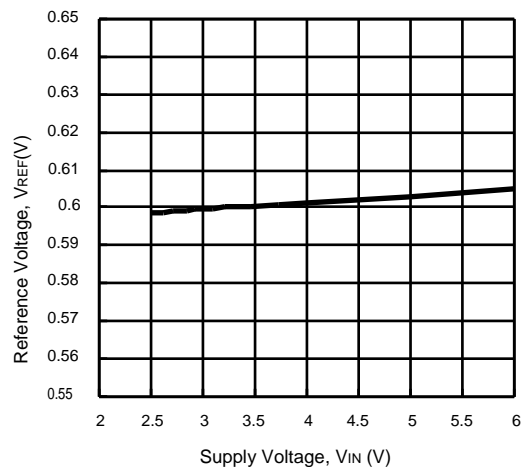
Supply Voltage vs. Quiescent Current



Supply Voltage vs. ON Resistance

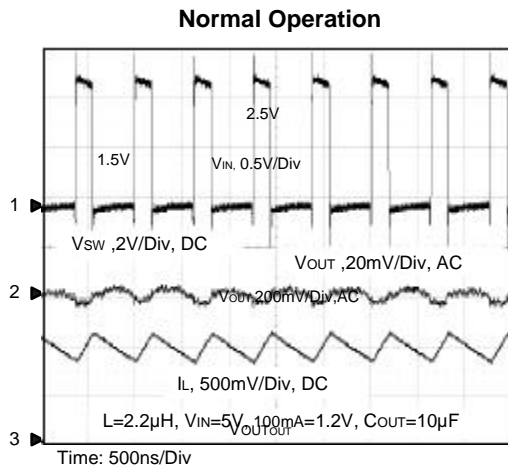
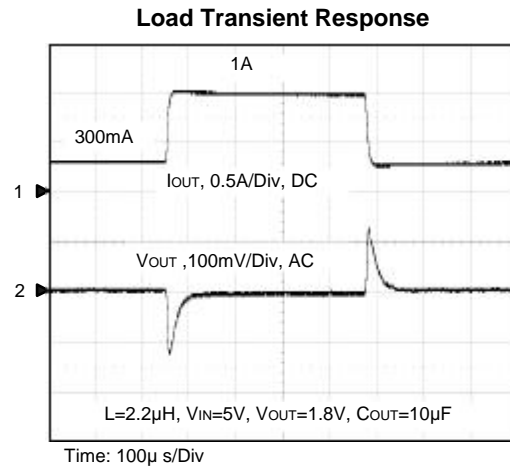
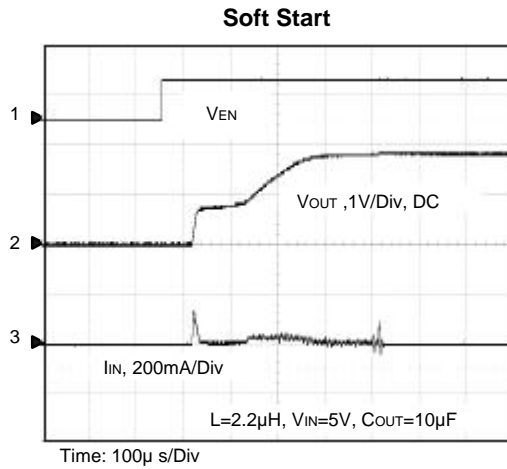


Supply Voltage v.s. Reference Voltage



## Operating Waveforms

(Refer to the application circuit in the section "Typical Application Circuits",  $V_{IN}=3.6V$ ,  $V_{OUT}=1.8V$ ,  $T_A=25^{\circ}C$  unless otherwise specified)



# JTMA7176

## Pin Description

PIN		FUNCTION
NO.	NAME	
1	EN1	Channel 1 Enable Control Input. Drive EN1 above 1V to turn on the Channel 1. Drive EN1 below 0.4V to turn it off. In shutdown situation, all functions are disabled to decrease the supply current below 1mA. Don't left this pin floating.
2	FB1	Channel 1 Feedback Input. Connect FB1 to the center point of the external resistor divider. The feedback voltage is 0.6V.
3	IN2	Channel 2 Supply Input. Bypass to the GND2 with a 4.7μF or greater ceramic capacitor.
4	GND2	Ground 2. Connected the exposed pad to the GND2.
5	SW2	Channel 2 Power Switch Output. Inductor connection to drains of the internal PMOSFET and NMOSFET switches.
6	EN2	Channel 2 Enable Control Input. Drive EN2 above 1V to turn on the Channel 2. Drive EN2 below 0.4V to turn it off. In shutdown situation, all functions are disabled to decrease the supply current below 1mA. Don't left this pin floating.
7	FB2	Channel 2 Feedback Input. Connect FB2 to the center point of the external resistor divider. The feedback voltage is 0.6V.
8	IN1	Channel 1 Supply Input. Bypass to the GND1 with a 4.7μF or greater ceramic capacitor.
9	GND1	Ground 1. Connected the exposed pad to the GND1.
10	SW1	Channel 1 Power Switch Output. Inductor connection to drains of the internal PMOSFET and NMOSFET switches.
Exposed Pad	NC	No Internal Connection. Connecting this pad to GND1 and GND2.

## Block Diagram

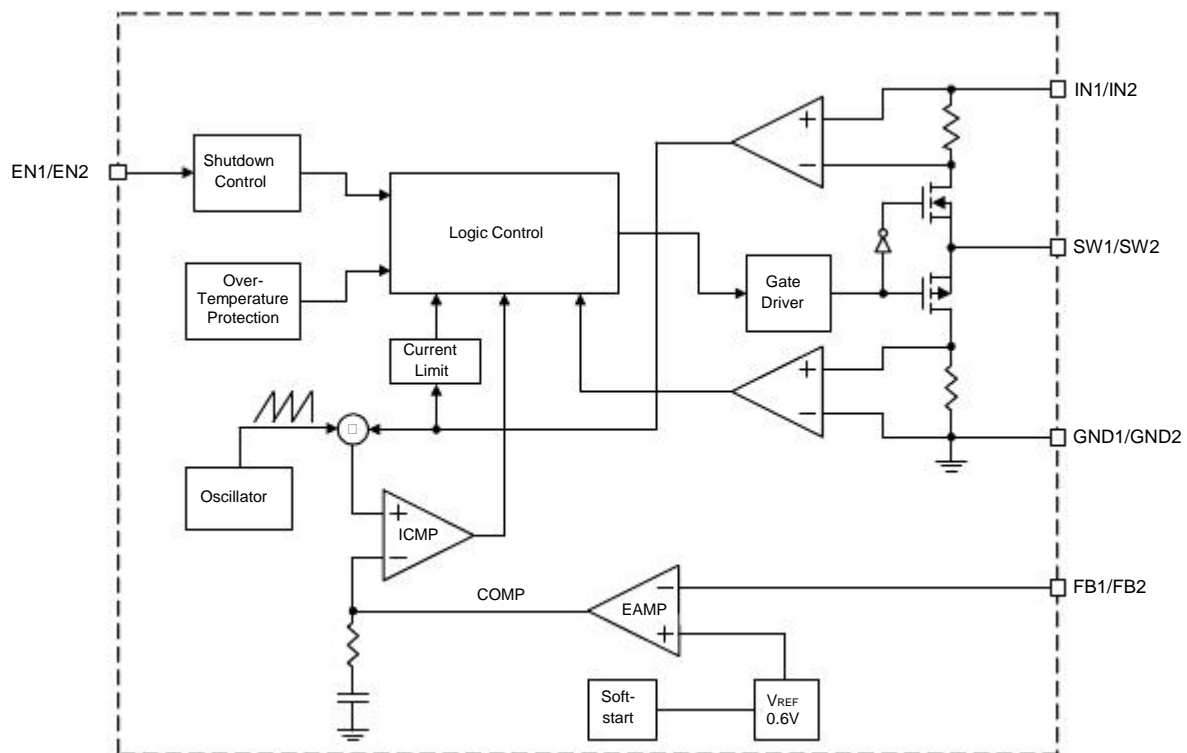
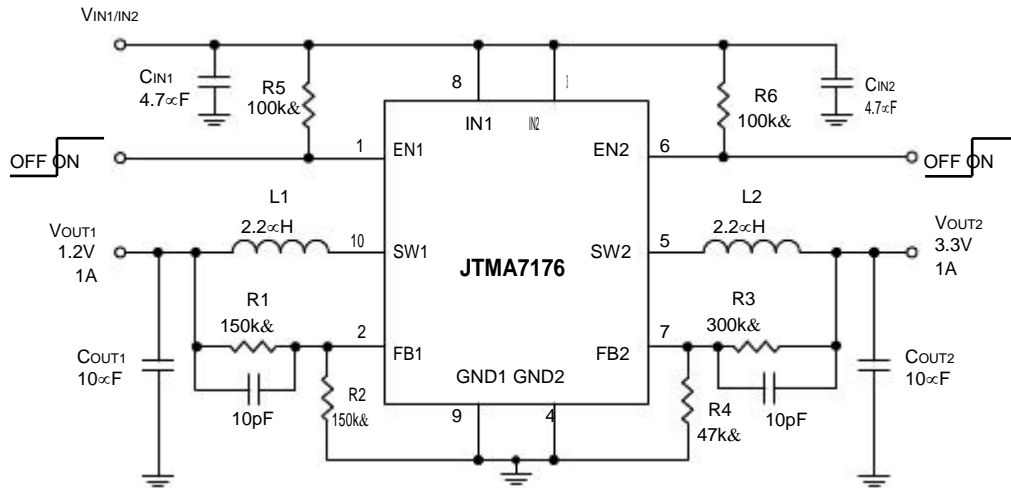


Diagram Represents 1/2 of the JTMA7176

# JTMA7176

## Typical Application Circuit



## Function Description

### Main Control Loop

The JTMA7176 has dual independent constant frequency, current-mode PWM step-down converters. During normal operation, the internal P-channel power MOSFET is turned on each cycle when the oscillator sets an internal RS latch and is turned off when an internal comparator (ICMP) resets the latch. The peak inductor current at which ICMP resets the RS latch is controlled by the voltage on the COMP, which is the output of the error amplifier (EAMP). An external resistive divider connected between  $V_{OUT}$  and ground allows the EAMP to receive an output feedback voltage  $V_{FB}$  at FB pin. When the load current increases, it causes a slightly decrease in  $V_{FB}$  associated with the 0.6V reference, which in turn causes the COMP voltage to increase until the average inductor current matches the new load current.

### Soft-Start

Each channel in the JTMA7176 has a built-in soft-start to control the output voltage rise during start-up. During soft-start, an internal ramp, connected to the one of the positive inputs of the error amplifier, raise up to replace the reference voltage (0.6V typical) until the ramp voltage reaches the reference voltage.

### Short Circuit Protection

For each channel, when the output is shortened to the ground, the frequency of the oscillator will be reduced to 210kHz. This lower frequency allows the inductor current to safely discharge, thereby preventing current runaway. The oscillator's frequency will gradually increase to its designed rate when the feedback voltage on the FB again approaches 0.6V.

### Over-Temperature Protection (OTP)

For each channel, the over-temperature circuit limits the junction temperature of the JTMA7176. When the junction temperature exceeds 150°C, a thermal sensor turns off the power MOSFETs, allowing the channels to cool down. The thermal sensor allows the converter to start a soft-start process and to regulate the output voltage again after the junction temperature cools by 40°C. The OTP is designed with a 40°C hysteresis to lower the average

Junction Temperature ( $T_J$ ) during continuous thermal overload conditions, increasing the lifetime of the device.

### Enable/Shutdown

For each channel, driving EN to the ground places the channel in shutdown mode. When in shutdown, the internal power MOSFETs are turned off, all internal circuitry shuts down, and the quiescent supply current reduces to 1mA maximally.

### Automatic PFM/PWM mode Switch

The JTMA7176 is a fixed frequency PWM peak current modulation control step-down converter. At light loads, the JTMA7176 will automatically enter in pulse frequency modulation operation to reduce the dominant switching losses. In PFM operation, the inductor current may reach zero or reverse on each pulse. A zero current comparator turns off the N-channel synchronous MOSFET, forcing DCM (Discontinuous Current Mode) operation at light load. These controls get very low quiescent, help to maintain high efficiency over the complete load range.



## Application Information

### Inductor Selection

Due to the high switching frequency as 1.5MHz, the inductor value of the application of the JTMA7176 is usually in the range from  $1\mu\text{H}$  to  $4.7\mu\text{H}$ . The criterion of selecting a suitable inductor depends on its maximum current ripple. The maximum current ripple defines as 40% of the fully load current. In the JTMA7176 applications, the maximum value of current ripple is 400mA, the 40% of 1A. Calculate L by the equation (1):

$$L = \frac{(V_{IN} - V_{OUT}) \cdot I_{OUT} \cdot \Delta I_L}{V_{IN} \cdot f_{osc} \cdot \Delta I_L} \dots\dots\dots(1)$$

where  $f_{osc}$  is the switching frequency of JTMA7176 and  $\Delta I_L$  is the value of the maximum current ripple. It can be any value of current ripple that smaller than the maximum value you can accept. In order to perform high efficiency, selecting a low DC resistance inductor is a helpful way. Another important parameter is the DC current rating of the inductor. The minimum value of DC current rating equals the full load value of 1A, and then plus the half of the current ripple. Choose inductors with suitable DC current rating to ensure the inductors don't operate in the saturation.

### Input Capacitor Selection

The input capacitor must be able to support the maximum input operating voltage and maximum RMS input current. The Buck converter absorbs pulse current from input power source.

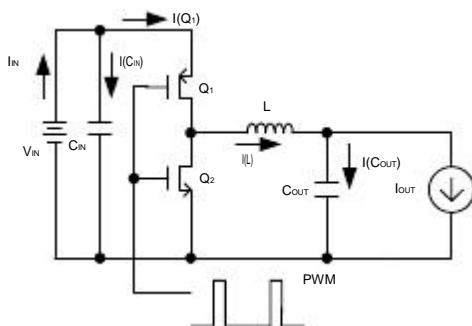


Figure-1

Figure-1 shows a schematic of a Buck converter. The waveforms are shown as Figure-2.

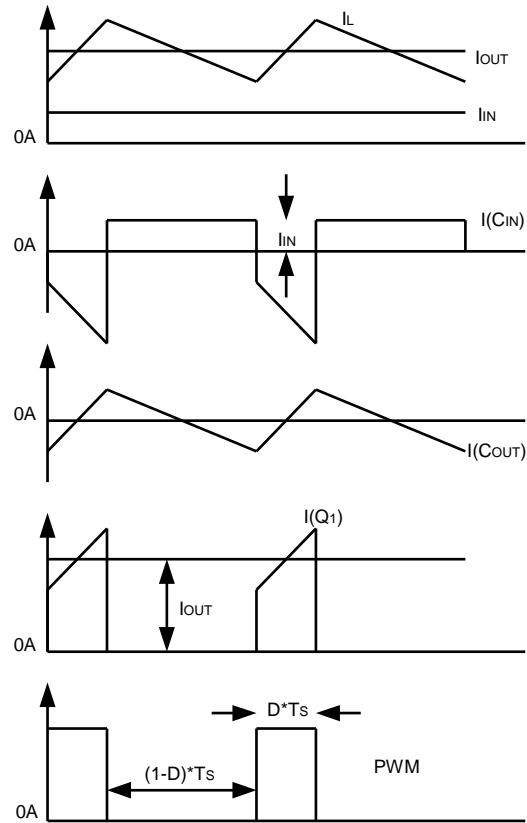


Figure-2

By observing the waveform of  $I(C_{IN})$ , the RMS value of  $I(C_{IN})$  is

$$I(C_{IN}) = \sqrt{I_{OUT}^2 \cdot D + I_{OUT}^2 \cdot (1-D)^2} \dots\dots(2)$$

Replace D and  $I_{IN}$  by following relation:

$$D = \frac{V_{OUT}}{V_{IN}} \dots\dots\dots(3)$$

$$I_{IN} = D \cdot I_{OUT} \dots\dots\dots(4)$$

The RMS value of input capacitor current equal:

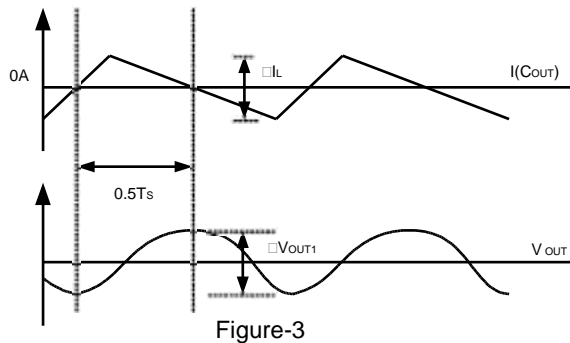
$$I(C_{IN}) = I_{OUT} \cdot D \cdot \sqrt{1/D} \dots\dots\dots(5)$$

When  $D=0.5$ , the RMS current of input capacitor will be maximum value. Use this value to choose the input capacitor with suitable current rating.

## Application Information (Cont.)

### Output Capacitor Selection

The output voltage ripple is a significant parameter to estimate the performance of a convertor. There are two discrete components that affect the output voltage ripple to be bigger or smaller. It is recommended to use the criterion mentioned in the "Inductor Selection" to choose a suitable inductor. Then, based on this known inductor current ripple, the value and equivalent-series-resistance (ESR) of output capacitor will affect the output voltage ripple to be smaller or larger. The output voltage ripple consists of two portions, one is the product of ESR and inductor current ripple, the other portion is the function of the inductor current ripple and the output capacitance. Figure-3 illustrates the waveform of the ripple voltage which is generated when the inductor ripple current charges or discharges the pure capacitor without the ESR.



Evaluate the  $\Delta V_{OUT1}$  by the ideal of energy equalization. According to the definition of Q,

$$Q = \frac{1}{2} \left( \frac{1}{\Delta I_L} + \frac{1}{2} \right) T_s = C_{OUT} \Delta V_{OUT1} \dots (6)$$

where  $T_s$  is the inverse of switching frequency and the  $\Delta I_L$  is the inductor current ripple. Move the  $C_{OUT}$  to the left side to estimate the value of  $\Delta V_{OUT1}$  as equation (7).

$$\Delta V_{OUT1} = \frac{\Delta I_L \oplus T_s}{8 \oplus C_{OUT}} \dots (7)$$

As mentioned above, one part of output voltage ripple is the product of the inductor current ripple and ESR of output capacitor. The equation (8) explains the output voltage ripple estimation.

$$\Delta V_{OUT} = \Delta I_L \oplus \left( ESR + \frac{T_s}{8 \oplus C_{OUT}} \right) \dots (8)$$

### Thermal Consideration

JTMA7176 is a high efficiency switching converter, it means less power loss transferred into heat. Due to the on resistance difference between internal power PMOSFET and NMOSFET, the power dissipation at high duty cycle is greater than the low duty cycle. The worst case in the dropout operation is the conduction loss dissipate mainly on the internal power PMOSFET. The power dissipation is nearly defined as:

$$P_D = (I_{OUT})^2 [R_{DS(P)} \oplus D + R_{DS(N)} \oplus (1 \ominus D)] \dots (9)$$

The JTMA 7176 provides internal over-temperature protection. When the junction temperature reaches 150 degrees centigrade, the JTMA7176 will turn off both internal power PMOSFET and NMOSFET. The estimation of the junction temperature,  $T_J$ , is defined as:

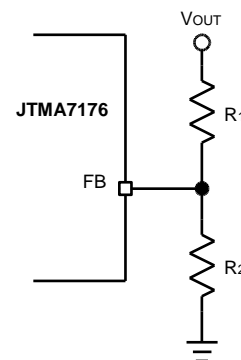
$$T_J = P_D \oplus \theta_{JA} \dots (10)$$

where the  $\theta_{JA}$  is the thermal resistance of the package utilized by the JTMA7176.

### Output Voltage Setting

Then JTMA7176 has the adjustable version for output voltage setting by the users. A suggestion of maximum value of  $R_2$  is 300k $\Omega$  to keep the minimum current that provides enough noise rejection ability through the resistor divider. The output voltage is programmed by the equation as below:

$$V_{OUT} = 0.6 \oplus \left( 1 + \frac{R_1}{R_2} \right) \dots (11)$$



## Application Information (Cont.)

### Layout Consideration

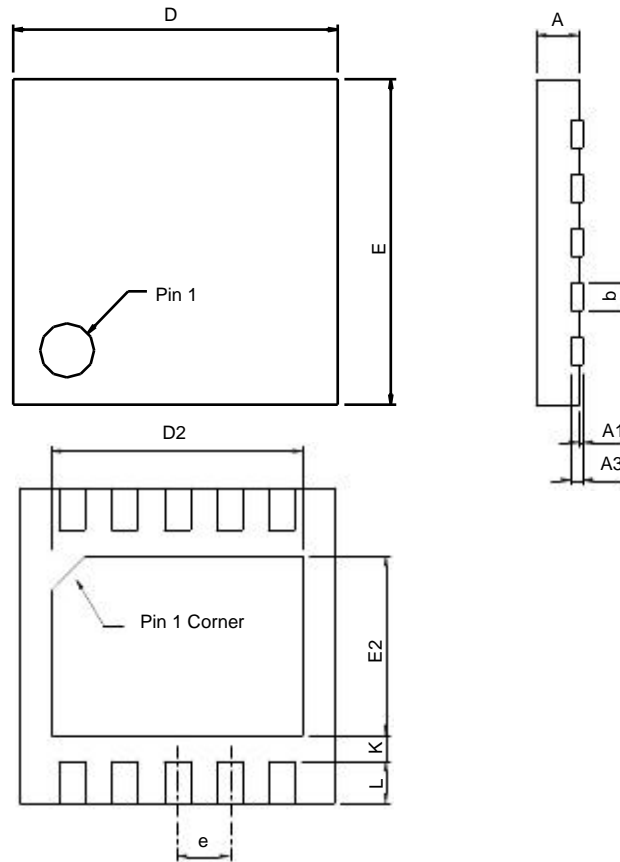
For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor should be placed close to the VIN and the GND. Connecting the capacitor and VIN/GND with short and wide trace without any via holes for good input voltage filtering.
2. The high current paths (GND1/GND2, IN1/IN2, and SW1/SW2) should be placed very close to the device with short, direct and wide traces.
3. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the SW pin to minimize the noise coupling into other circuits.
4. Since the feedback pin and network is a high impedance circuit, the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.
5. A star ground connection or ground plane minimizes ground shifts and noise is recommended.

# JTMA7176

## Package Information

TDFN3x3-10

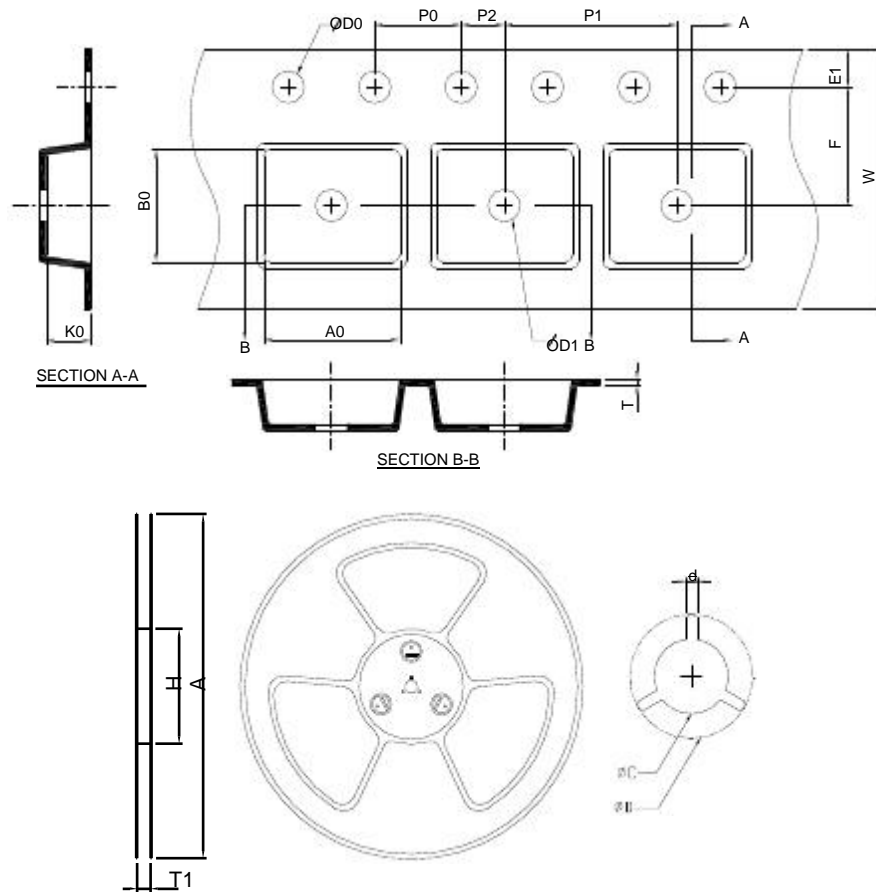


S Y M B O L	TDFN3x3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-229 VEED-5.

# JTMA7176

## Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN3x3-10	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

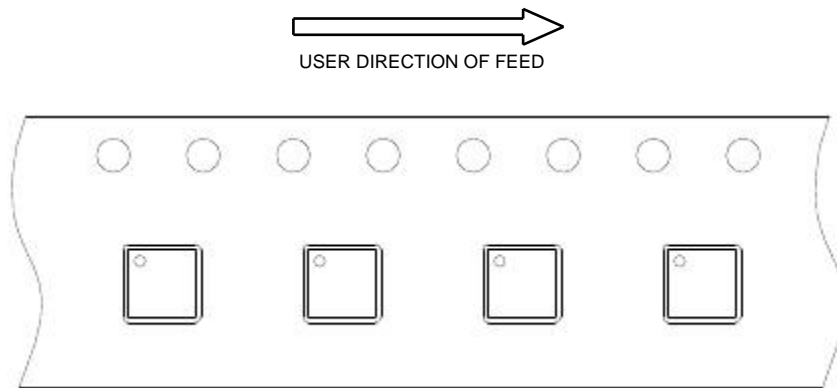
(mm)

## Devices Per Unit

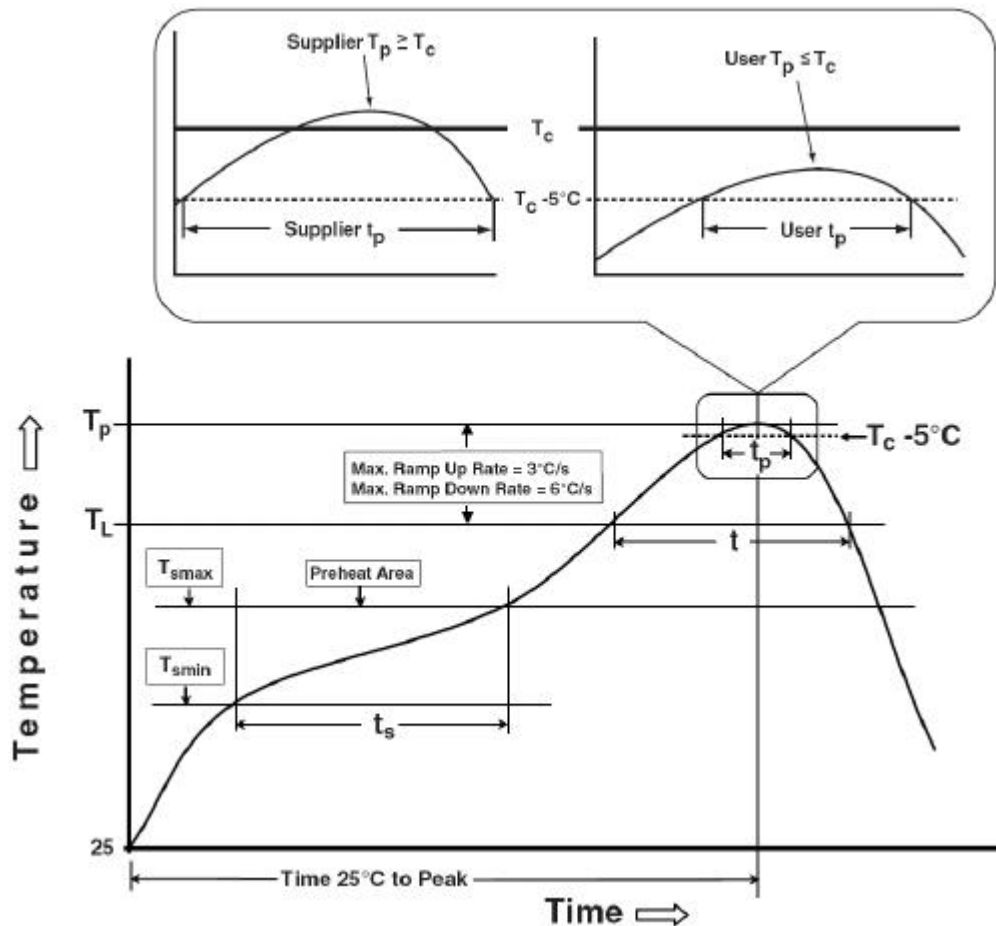
Package Type	Unit	Quantity
TDFN3x3-10	Tape & Reel	3000

## Taping Direction Information

TDFN3x3-10



## Classification Profile



## Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
<b>Preheat &amp; Soak</b> Temperature min ( $T_{smin}$ ) Temperature max ( $T_{smax}$ ) Time ( $T_{smin}$ to $T_{smax}$ ) ( $t_s$ )	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate ( $T_{smax}$ to $T_P$ )	3 °C/second max.	3°C/second max.
Liquidous temperature ( $T_L$ ) Time at liquidous ( $t_L$ )	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature ( $T_P$ )*	See Classification Temp in table 1	See Classification Temp in table 2
Time ( $t_P$ )** within 5°C of the specified classification temperature ( $T_C$ )	20** seconds	30** seconds
Average ramp-down rate ( $T_P$ to $T_{smax}$ )	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature ( $T_P$ ) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature ( $t_P$ ) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures ( $T_C$ )

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> ε350
<2.5 mm	235 °C	220 °C
ε2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures ( $T_C$ )

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> 350-2000	Volume mm <sup>3</sup> >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
ε2.5 mm	250 °C	245 °C	245 °C

## Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ $T_j=125^{\circ}\text{C}$
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≥ 2KV
MM	JESD-22, A115	VMM ≥ 200V
Latch-Up	JESD 78	10ms, $1_{tr} \geq 100\text{mA}$

## Customer Service