JTMA7325

5A 5V 1MHz Synchronous Buck Converter

Features

- **High Efficiency up to 95%**
  - Automatic PFM/PWM Mode Operation
- **Adjustable Output Voltage from 0.6V to V_{PVDD}**
- **Integrated 65m& High Side / 55m& Low Side MOSFETs**
- **Low Dropout Operation: 100% Duty Cycle**
- **Stable with Low ESR Ceramic Capacitors**
- **Power-On-Reset Detection on VDD and PVDD**
- **Integrated Soft-Start and Soft-Stop**
- **Over-Temperature Protection**
- **Over-Voltage Protection**
- **Under-Voltage Protection**
- **High/ Low Side Current Limit**
- **Power Good Indication**
- **Enable/Shutdown Function**
- **Small SOP-8P Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **Notebook Computer & UMPC**
- **LCD Monitor/TV**
- **Set-Top Box**
- **DSL, Switch HUBr**
- **Portable Instrument**

General Description

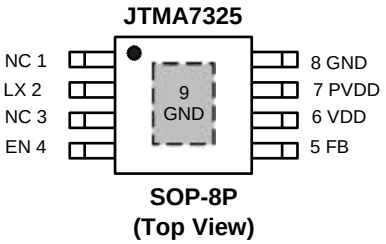
JTMA7325 is a 5A synchronous buck converter with integrated 65m & high side and 55m & low side power MOSFETs. The JTMA7325, design with a current-mode control scheme, can convert wide input voltage of 2.6V to 6V to the output voltage adjustable from 0.6V to 6V to provide excellent output voltage regulation.

The JTMA7325 is equipped with an automatic PFM/PWM mode operation. At light load , the IC operates in the PFM mode to reduce the switching losses. At heavy load, the IC works in PWM mode. At PWM mode, the switching frequency is set by the external resistor.

The JTMA7325 is also equipped with Power-on-reset, soft-start, soft-stop, and whole protections (under-voltage, over-voltage, over-temperature and current-limit) into a single package.

This device, available SOP-8P, provides a very compact system solution external components and PCB area.

Pin Configuration



SOP-8P
(Top View)

Exposed pad
The pin 6 must be connected to the pin 9 (exposed pad)

Ordering and Marking Information

JTMA7325 Assembly Material Handling Code Temperature Range Package Code		Package Code KA : SOP-8P Operating Ambient Temperature Range I : -40 to 85℃ Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
JTMA7325 KA :	JTMA7325 XXXXX	XXXXX - Date Code

Note: JIATAIMU lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. JIATAIMU lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. JIATAIMU defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{PVDD}, V_{VDD}	Input Supply Voltage		-0.3 ~ 6.5	V
V_{LX}	LX to GND Voltage	<30ns pulse width	-3 ~V_{PVDD}+3	V
		>30ns pulse width	-1 ~V_{PVDD}+0.3	V
	POK, FB, EN to GND Voltage		-0.3 ~ 6.5	V
P_D	Power Dissipation		Internally Limited	W
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds		260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2) SOP-8P	60	°C/W
θ_{JC}	Junction-to-Case Resistance in Free Air (Note 3) SOP-8P	20	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of SOP-8P is soldered directly on the PCB.

Note 3: The case temperature is measured at the center of the exposed pad on the underside of the SOP-8P package.

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_{VDD}	Control and Driver Supply Voltage	2.6 ~ 6	V
V_{PVDD}	Input Supply Voltage	2~6	V
V_{OUT}	Converter Output Voltage	0.6~6	V
L	Inductance	1 ~ 3.3	∝H
I_{OUT}	Converter Output Current	0~5	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 4: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{VDD}=V_{PVDD}=5V, V_{OUT}=3.3V, T_A=25₀C.

Symbo	Parameter	Test Conditions	APW7325			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{VDD}	VDD Supply Current	V_{FB}=0.7V	-	460	-	∝A
I_{VDD_SDH}	VDD Shutdown Supply Current	EN=GND	-	-	1	∝A
POWER-ON-RESET (POR)						
	VDD POR Voltage Threshold	V_{VDD} Rising	2.3	2.4	2.5	V
	VDD POR Hysteresis		-	0.2	-	V
	PVDD POR Voltage Threshold		1.5	1.7	1.9	V
	PVDD POR Hysteresis		-	0.2	-	V
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage		-	0.6	-	V
		All temperature	-1	-	+1	%
	Output Accuracy	I_{OUT}=10mA~5A, V_{VDD}=2.6~5V	-1.5	-	+1.5	%
OSCILLATOR AND DUTY CYCLE						
F_{OSC}	Oscillator Frequency		0.85	1	1.15	MHz
	Maximum Converter's Duty	V_{FB}=0.7V	-	100	-	%
	Minimum on Time		-	100	-	ns
POWER MOSFET						
	High Side P-MOSFET Resistance	V_{VDD}=5V, I_{LX}=0.5A, T_A=25°C	-	65	80	m&
	Low Side N-MOSFET Resistance	V_{VDD}=5V, I_{LX}=0.5A, T_A=25°C	-	55	75	m&
	High/Low Side MOSFET Leakage Current		-	-	10	∝A
CURRENT-MODE PWM CONVERTER						
Gm	Error Amplifier Transconductance		-	550	-	∝A/V
	Error Amplifier DC Gain		-	80	-	dB
	Current Sense Transresistance		-	400	-	m&
T_D	Dead Time		-	20	-	ns

Electrical Characteristics (Cont.)

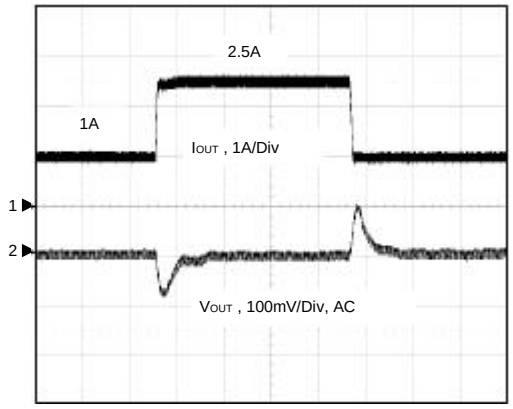
Unless otherwise specified, these specifications apply over V_{VDD}=V_{PVDD}=5V, V_{OUT}=3.3V, T_A=25°C.

Symbo	Parameter	Test Conditions	APW7325			Unit
			Min.	Typ.	Max.	
PROTECTIONS						
I_{LIM}	High Side MOSFET Current-Limit	Peak Current	6	6.5	8	A
T_{OTP}	Over-Temperature Trip Point		-	160	-	°C
	Over-Temperature Hysteresis		-	50	-	°C
	Over-Voltage Protection Threshold		120	-	135	$\%V_{REF}$
	Under-Voltage Protection Threshold		45	50	55	$\%V_{REF}$
SOFT-START, ENABLE, AND INPUT CURRENTS						
	Soft-Start Time		-	1	-	ms
	EN Enable Threshold		-	-	1.4	V
	EN Shutdown Threshold		0.5	-	-	V
	EN Pull Low Resistance		-	500	-	k&

Operating Waveforms

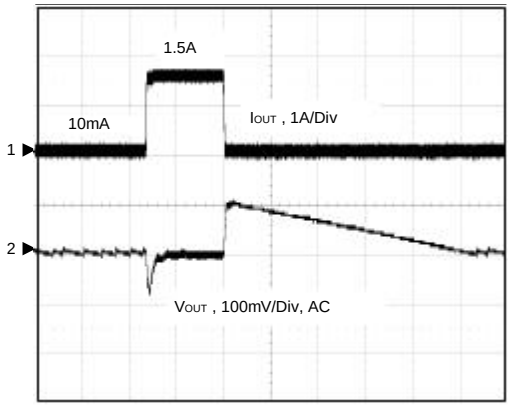
Refer to the typical application circuit. The test condition is V_{IN}=5V, T_A= 25oC unless otherwise specified.

Load Transient Response



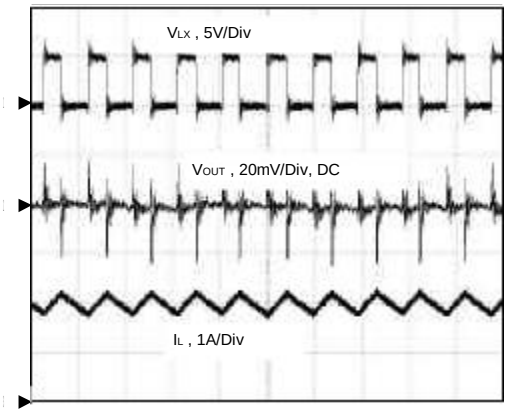
TIME: 20∝s/Div

Load Transient Response



TIME: 50∝s/Div

Normal Operating Waveform

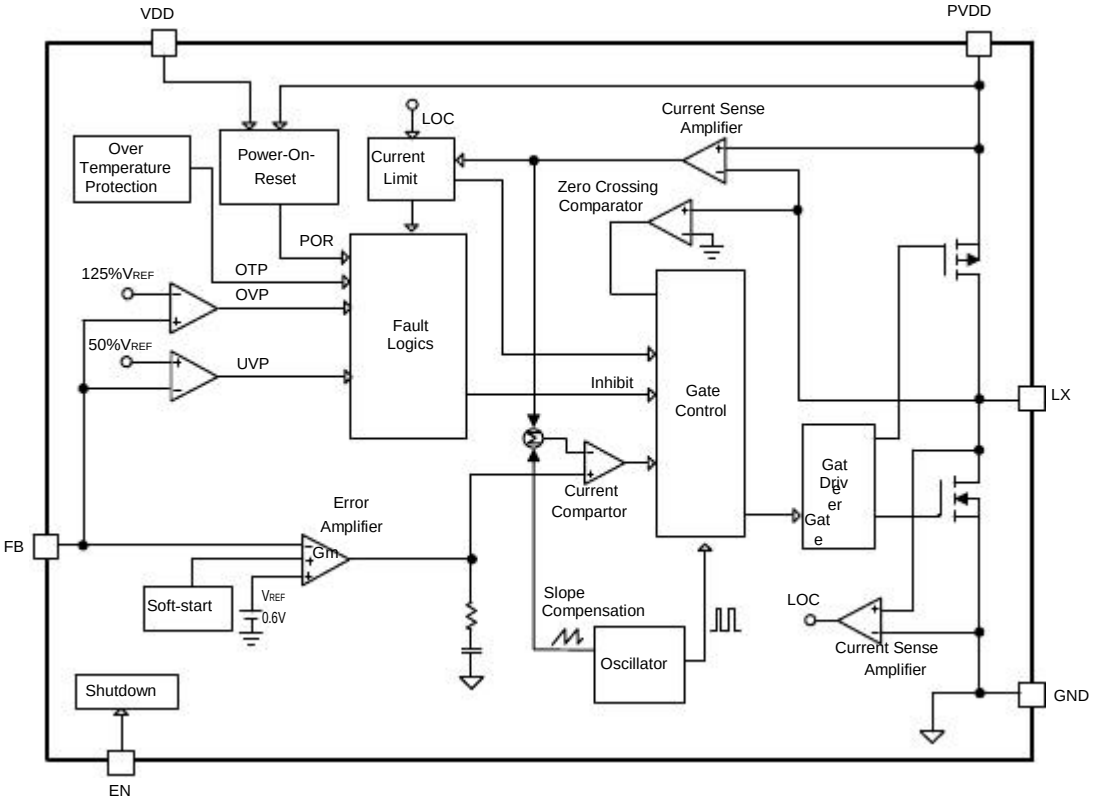


TIME: 1∝s/Div

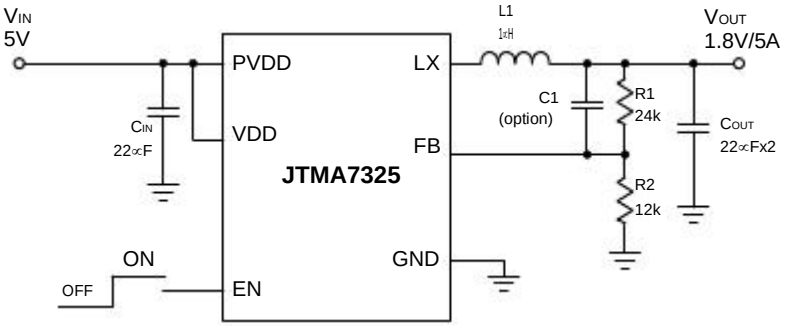
Pin Description

PIN		FUNCTION
NO.	NAME	
1,3	NC	No Connection.
2	LX	Power Switching Output. LX is the Junction of the high-side and low-side Power MOSFETs
4	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on
5	FB	Output Feedback Input. The APW7325 senses the feedback voltage via FB and regulates the voltage at 0.6V. Connecting FB with a resistor-divider from the converter's output sets the output voltage.
6	VDD	Signal Input. VDD supplies the control circuitry, gate drivers. Connecting a ceramic bypass capacitor from VDD to GND to eliminate switching noise and voltage ripple on the input to the IC.
7	PVDD	Power Input. PVDD supplies the step-down converter switches. Connecting a ceramic bypass capacitor from PVDD to GND to eliminate switching noise and voltage ripple on the input to the IC.
9	GND (Exposed Pad)	Ground and Exposed pad. Connect the exposed pad to the system ground plan with large copper area for dissipating heat into the ambient air.
8	GND	Ground. Power and signal ground.

Block Diagram



Typical Application Circuit



Function Description

VDD and PVDD Power-On-Reset (POR)

The JTMA7325 keeps monitoring the voltage on VDD and PVDD pins to prevent wrong logic operations which may occur when VDD or PVDD voltage is not high enough for internal control circuitry to operate. The VDD POR rising threshold is 2.4V (typical) with 0.2V hysteresis and PVDD POR rising threshold is 1.7V with 0.2V hysteresis. During start-up, the VDD and PVDD voltage must exceed the enable voltage threshold. Then, the IC starts a start-up process and ramps up the output voltage to the voltage target.

Output Under-Voltage Protection (UVP)

In the operational process, if a short-circuit occurs, the output voltage will drop quickly. Before the current-limit circuit responds, the output voltage will fall out of the required regulation range. The under-voltage continually monitors the FB voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold, the IC starts soft-stop function and shuts down converter's output.
The under-voltage threshold is 50% of the nominal output voltage. The under-voltage comparator has a built-in 3∝s noise filter to prevent the chips from wrong UVP shutdown being caused by noise. JTMA7325 will be latched after under-voltage protection.

Over-Voltage Protection (OVP)

The over-voltage function monitors the output voltage by FB pin. When the FB voltage increases over 125% of the reference voltage due to the high-side MOSFET failure or for other reasons, the over-voltage protection comparator will trigger soft-stop function and shutdown the converter output.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the JTMA7325. When the junction temperature exceeds T_J=+160°C, a thermal sensor turns off the both power MOSFETs, allowing the devices to cool. The thermal sensor allows the converters to start a start-up process and to regulate the output voltage again after the junction temperature cools by 50°C. The OTP is designed with a 50°C hysteresis to lower the average T_J during continuous thermal overload conditions, increasing lifetime of the JTMA7325.

Current-Limit Protection

The JTMA7325 monitors the output current, flows through the high-side and low-side power MOSFETs, and limits the current peak at current-limit level to prevent the IC from damaging during overload, short-circuit and over-voltage conditions. Typical high side power MOSFET current limit is 6.5A, and low side MOSFET current limit is 1.9A.

Soft-Start

The JTMA7325 has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during start-up. During soft-start, an internal voltage ramp connected to one of the positive inputs of the error amplifier, rises up to replace the reference voltage (0.6V) until the voltage ramp reaches the reference voltage. During soft-start without output over-voltage, the JTMA7325 converter's sinking capability is disabled until the output voltage reaches the voltage target.

Soft-Stop

At the moment of shutdown controlled by EN signal, under-voltage event or over-voltage event, the JTMA7325 initiates a soft-stop process to discharge the output voltage in the output capacitors. Certainly, the load current also discharges the output voltage. During soft-stop, the internal voltage ramp (V_{RAMP}) falls down to replace the reference voltage. Therefore, the output voltage falls down slowly at the light load. After the soft-stop interval elapses, the soft-stop process ends and the IC turns.

Enable and Shutdown

Driving EN to ground places the JTMA7325 in shutdown. In shutdown mode, the internal N-Channel power MOSFET turns off, all internal circuitry shuts down and the quiescent supply current reduces to less than 1∝A.

Application Information

Input Capacitor Selection

Because buck converters have a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering, minimizing the interference with other circuits caused by high input voltage spikes. Also, the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. For good input voltage filtering, usually a 22∝F input capacitor is sufficient. It can be increased without any limit for better input-voltage filtering. Ceramic capacitors show better performance because of the low ESR value, and they are less sensitive against voltage transients and spikes compared to tantalum capacitors. Place the input capacitor as close as possible to the input and GND pin of the device for better performance.

Inductor Selection

For high efficiencies, the inductor should have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. A reasonable starting point for setting ripple current, □I_L, is 40% of maximum output current. The recommended inductor value can be calculated as below:

$$L \varepsilon \frac{V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{F_{SW} \oplus \square I_L}$$

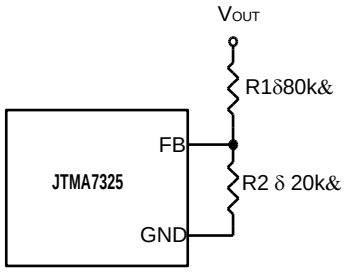
$$I_{L(MAX)} = I_{OUT(MAX)} + 1/2 \times \square I_L$$

To avoid the saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current.

Output Voltage Setting

In the adjustable version, the output voltage is set by a resistive divider. The external resistive divider is connected to the output, allowing remote voltage sensing as shown in “Typical Application Circuits”. A suggestion of maximum value of R2 is 20k& to keep the minimum current that provides enough noise rejection ability through the resistor divider. The output voltage can be calculated as below:

$$V_{OUT} = V_{REF} \oplus \left(1 + \frac{R1}{R2}\right) = 0.6 \oplus \left(1 + \frac{R1}{R2}\right)$$

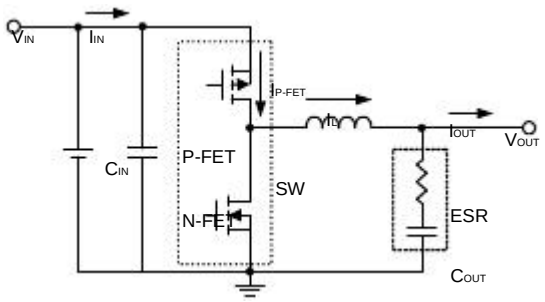


Output Capacitor Selection

The current-mode control scheme of the JTMA7325 allows the use of tiny ceramic capacitors. The higher capacitor value provides the good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

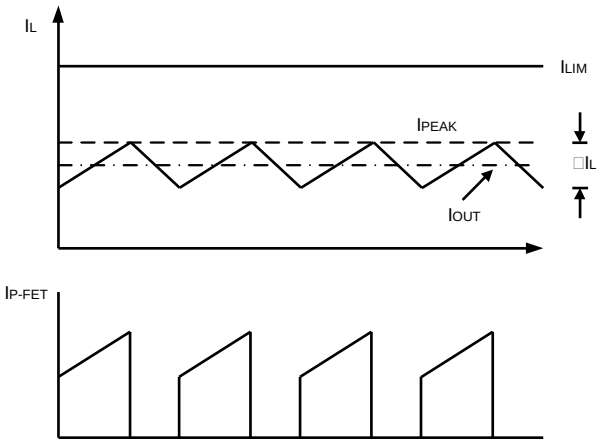
$$\square V_{OUT} \; E \; \frac{V_{OUT} \oplus \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{F_{SW} \oplus L_N} \oplus \left(ESR + \frac{1}{8 \oplus F_{SW} \oplus C_{OUT}}\right)$$

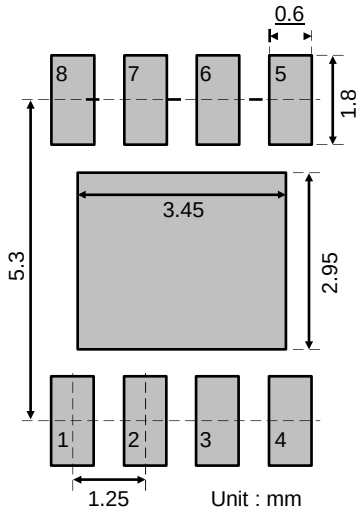
When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.



Application Information (Cont.)

Output Capacitor Selection (Cont.)





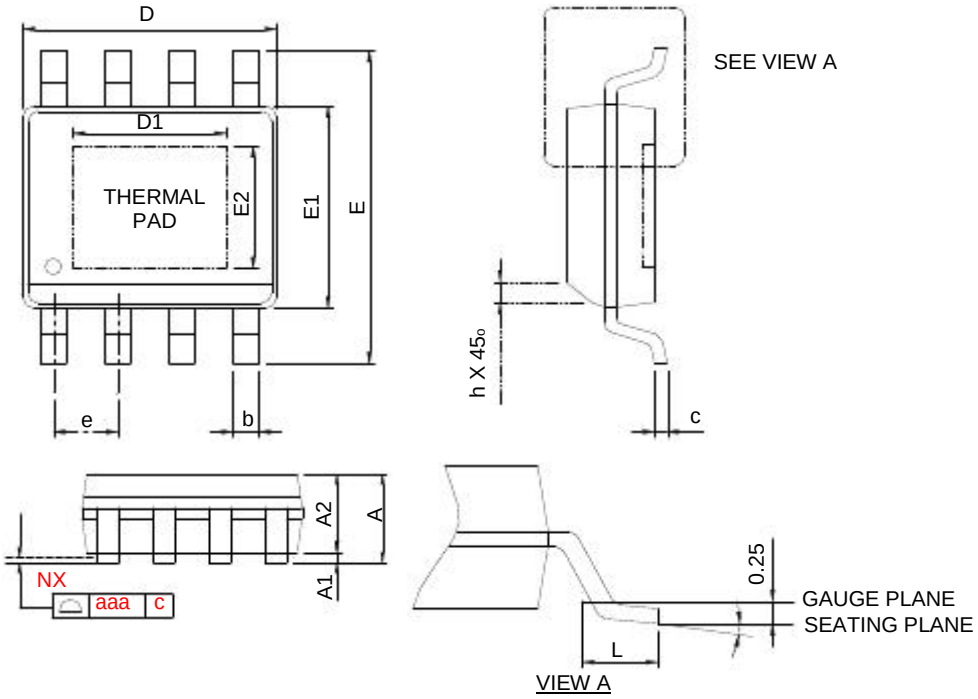
Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor should be placed close to the PVDD and GND. Connecting the capacitor and PVDD/GND with short and wide trace without any via holes for good input voltage filtering. The distance between VIN/GND to capacitor less than 2mm respectively is recommended.
2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the LX pin to minimize the noise coupling into other circuits.
3. The output capacitor should be place closed to LX and GND.
4. Since the feedback pin and network is a high impedance circuit the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.
5. A star ground connection or ground plane minimizes ground shifts and noise is recommended.

Package Information

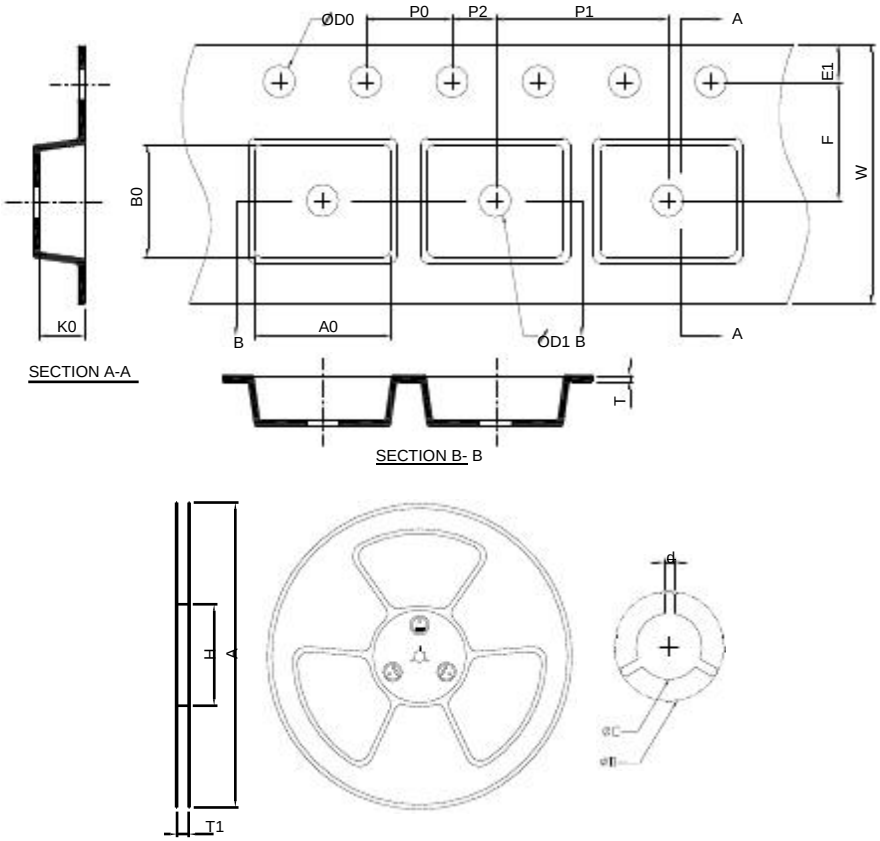
SOP-8P



SYMBOL	SOP-8P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.60		0.063
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
D1	2.50	3.50	0.098	0.138
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
0	0°C	8°C	0°C	8°C
aaa	0.10		0.004	

Note : 1. Followed from JEDEC MS-012 BA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-8P	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

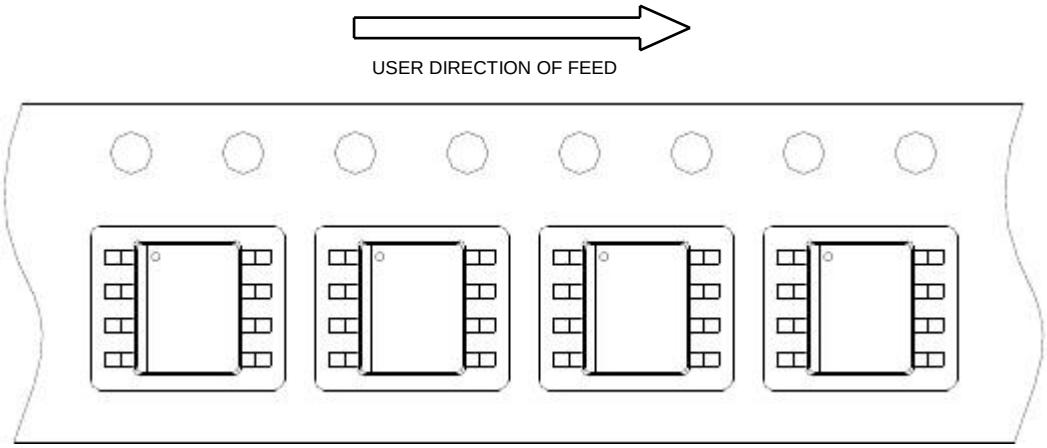
(mm)

Devices Per Unit

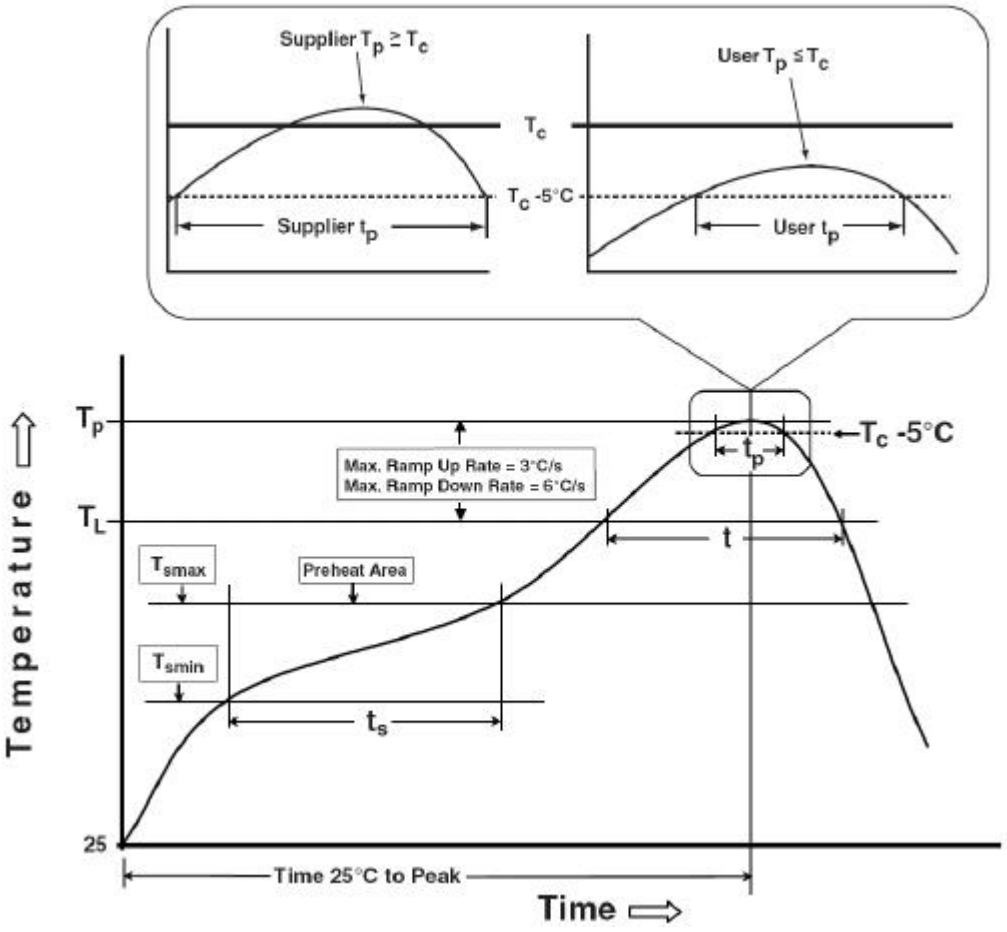
Package Type	Unit	Quantity
SOP-8P	Tape & Reel	2500

Taping Direction Information

SOP-8P



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ε350
<2.5 mm	235 °C	220 °C
ε2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
ε2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_J=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

Customer Service