

## Dual N-Channel Enhancement Mode Power MOSFET

**DESCRIPTION**

The JTM4840 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

**GENERAL FEATURES**

•  $V_{DS} = 40V, I_D = 7.0A$

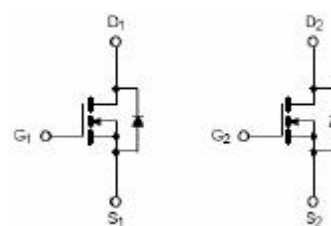
$R_{DS(ON)} < 24m\Omega @ V_{GS}=10V$

$R_{DS(ON)} < 38m\Omega @ V_{GS}=4.5V$

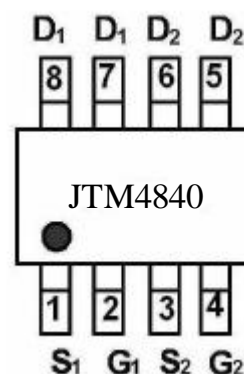
- High density cell design for ultra low  $R_{dson}$
- Fully characterized Avalanche voltage and current

**Application**

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



Schematic diagram



Marking and pin Assignment



SOP-8 top view

**Package Marking And Ordering Information**

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
JTM4840	JTM4840	SOP-8	Ø330mm	12mm	2500 units

**Absolute Maximum Ratings (TA=25°C unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	±20	V
Drain Current-Continuous	$I_D$	7	A
Drain Current-Continuous( $T_A=100^\circ C$ )	$I_D (100^\circ C)$	5	A
Pulsed Drain Current	$I_{DM}$	30	A
Maximum Power Dissipation	$P_D$	3	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	°C

**Thermal Characteristic**

Thermal Resistance, Junction-to-Ambient(Note 2)	$R_{\theta JA}$	42	°C/W
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**Electrical Characteristics (TA=25°C unless otherwise noted)**

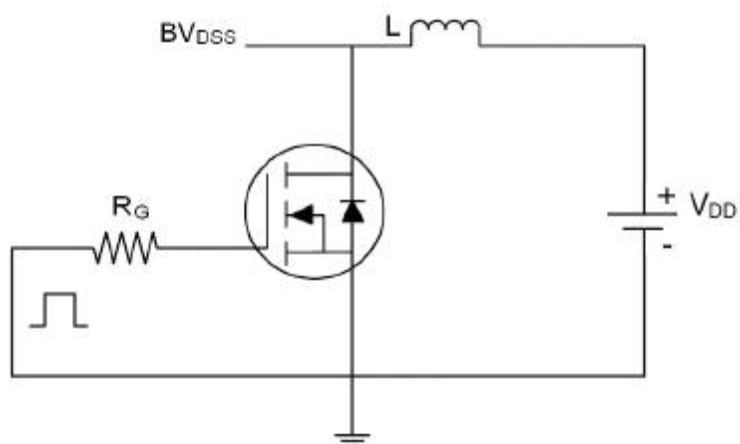
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	30	33	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1	1.3	2.2	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =7A	-	18.5	24	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A	-	27	38	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =7A	5	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, F=1.0MHz	-	2100	-	PF
Output Capacitance	C <sub>oss</sub>		-	460	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	230	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =10V, I <sub>D</sub> =7A V <sub>GS</sub> =10V, R <sub>GEN</sub> =2.7Ω	-	20	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	15	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	60	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	10	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =7A, V <sub>GS</sub> =10V	-	41	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	14	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	11	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =7A	-	-	1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	7	A

**Notes:**

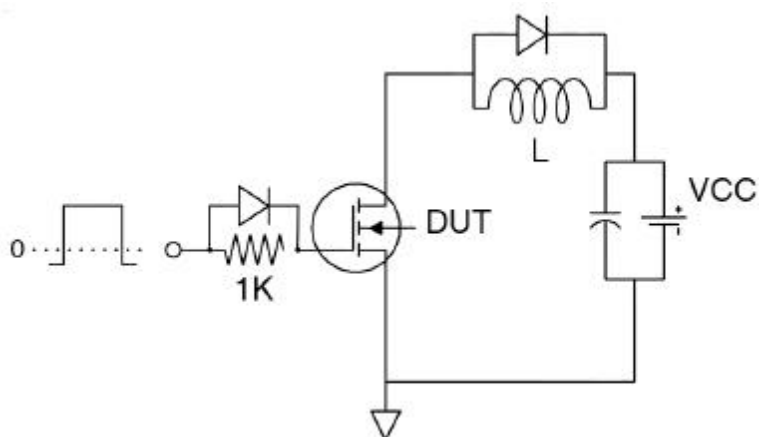
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

## Test circuit

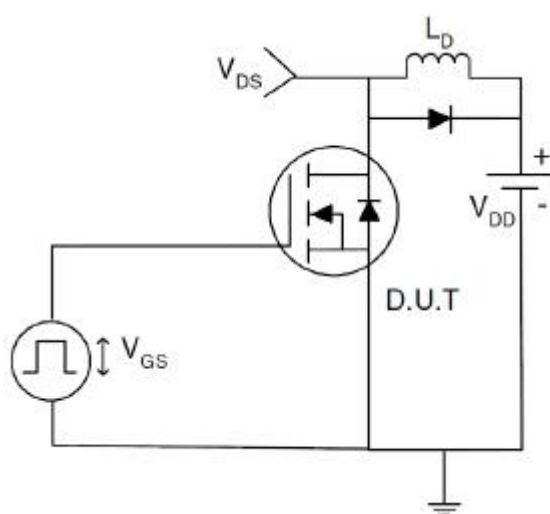
### 1) EAS test Circuits



### 2) Gate charge test Circuit:



### 3) Switch Time Test Circuit:



## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

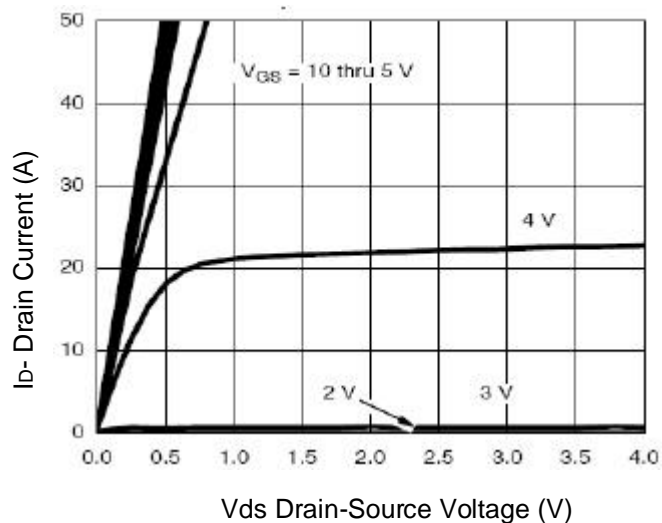


Figure 1 Output Characteristics

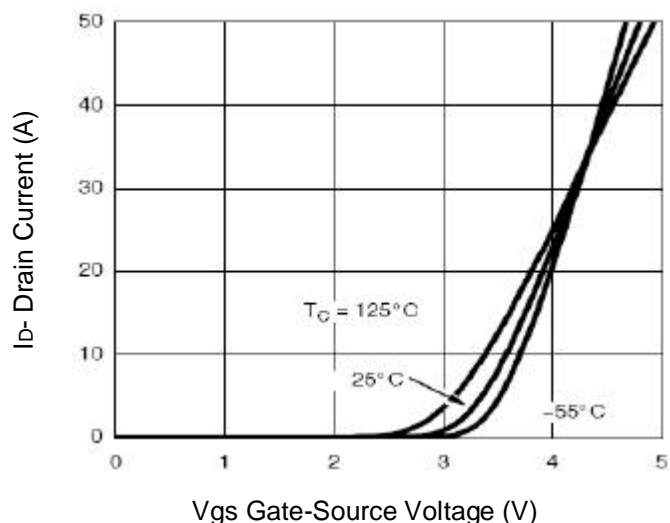


Figure 2 Transfer Characteristics

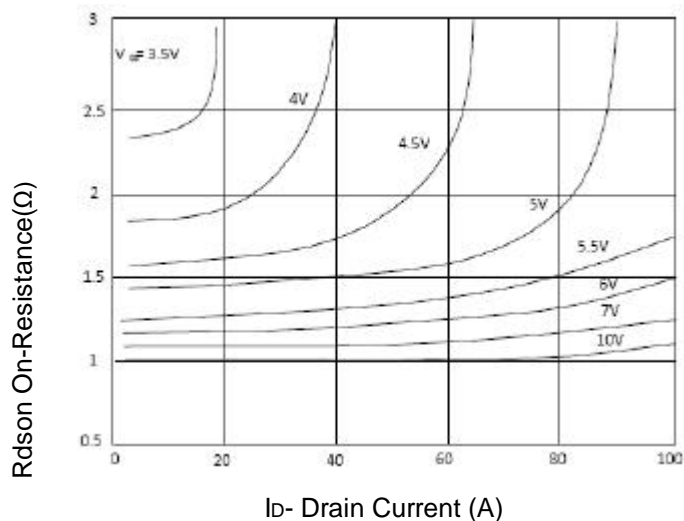


Figure 3 Rdson- Drain Current

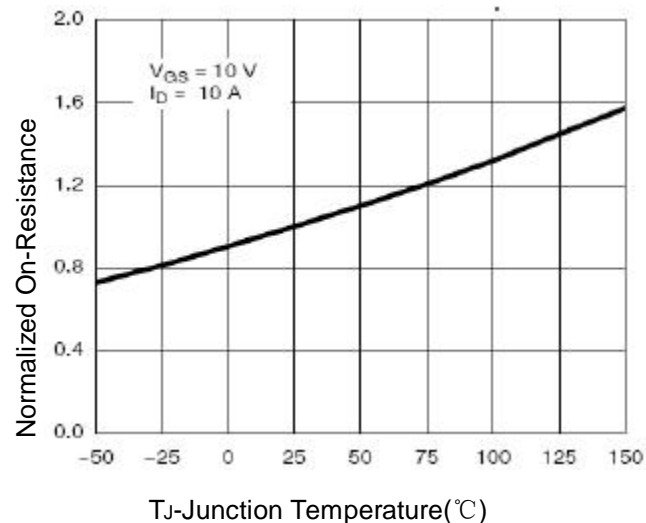


Figure 4 Rdson-Junction Temperature

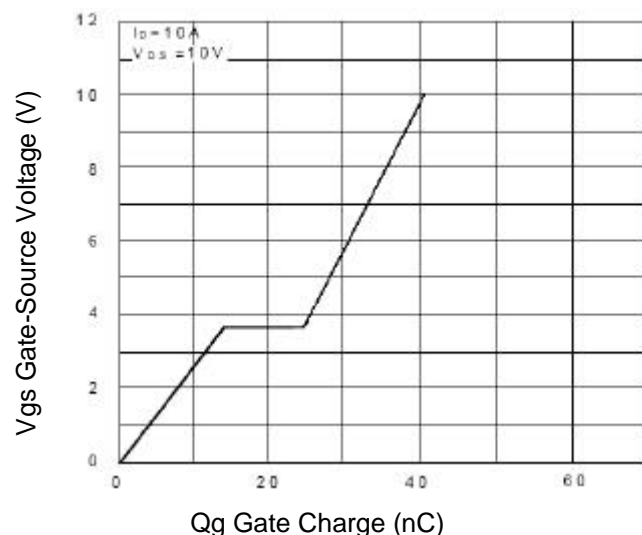


Figure 5 Gate Charge

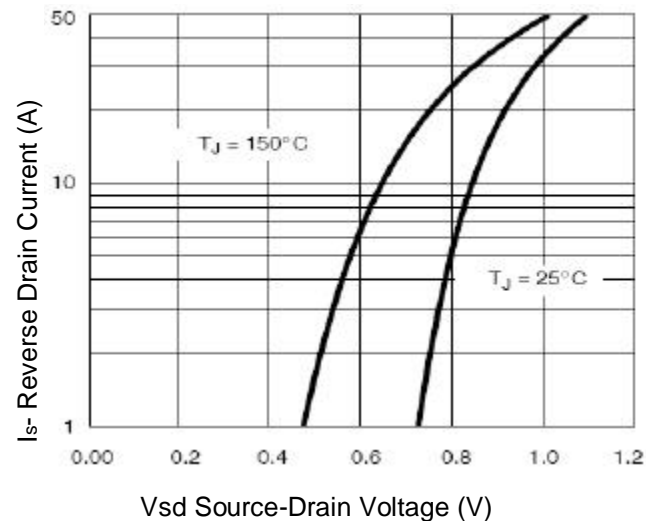


Figure 6 Source- Drain Diode Forward

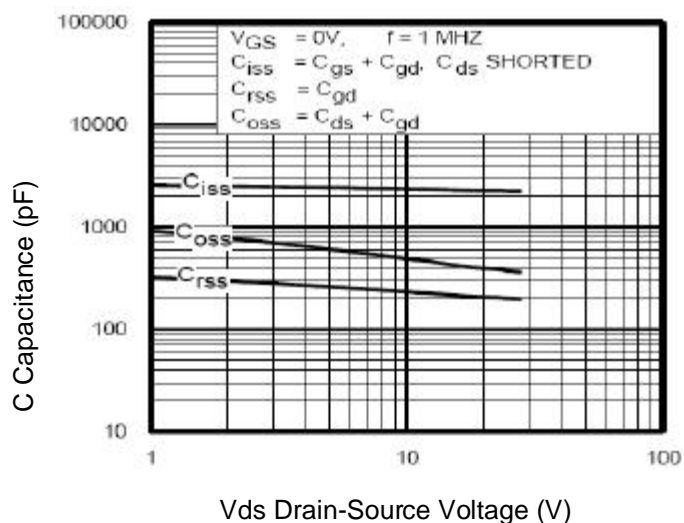
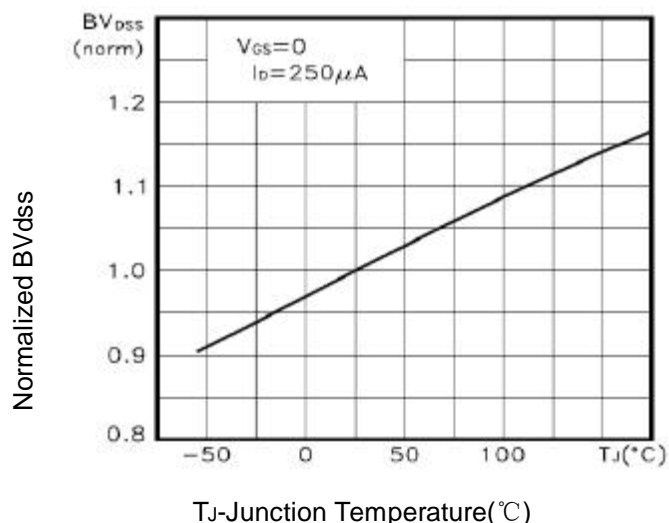
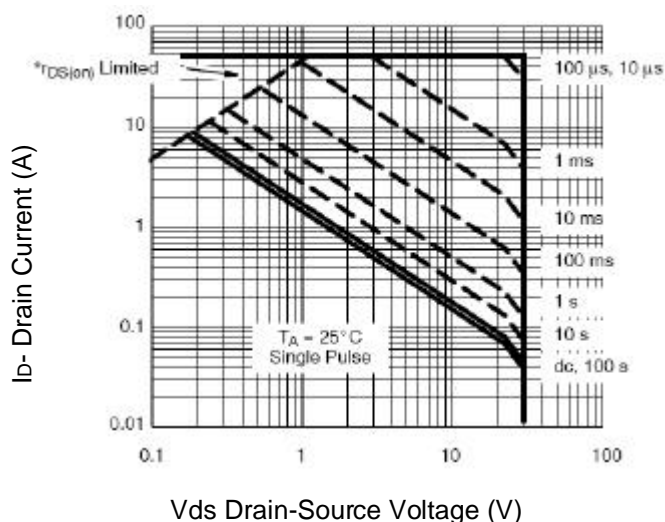
Figure 7 Capacitance vs  $V_{ds}$ Figure 9  $BV_{dss}$  vs Junction Temperature

Figure 8 Safe Operation Area

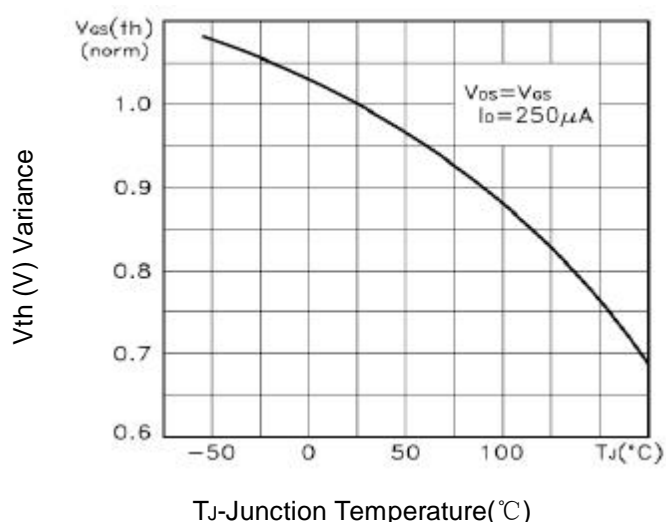
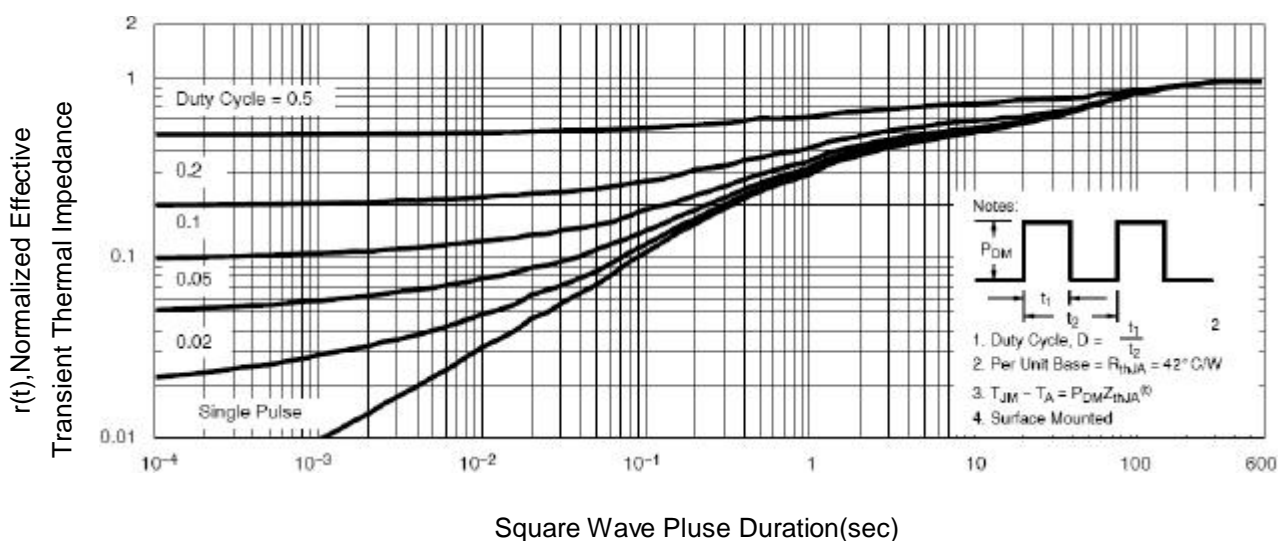
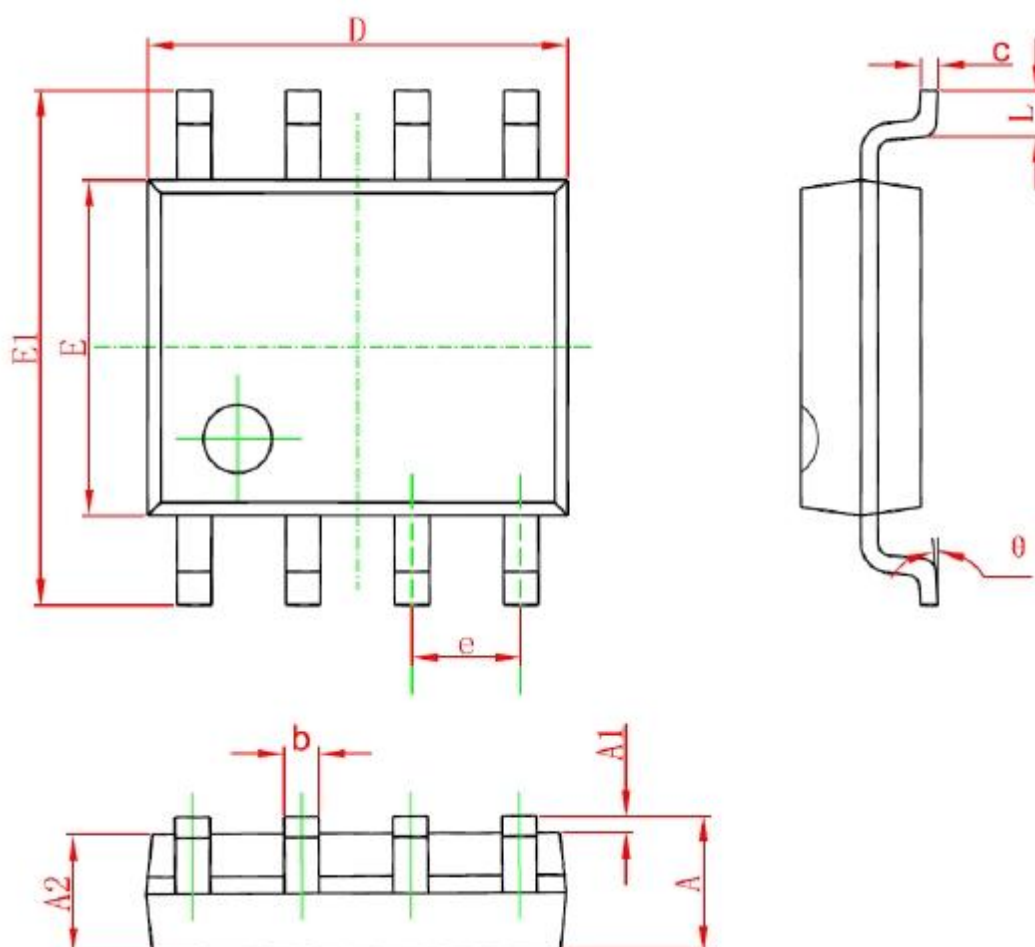
Figure 10  $V_{GS(th)}$  vs Junction Temperature

Figure 11 Normalized Maximum Transient Thermal Impedance

## SOP-8 PACKAGE IN FORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°

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