
Dual Channel Synchronous Buck DC/DC Converter

Features

- Up to 94% Efficiency
- Current Mode Operation for Excellent Line and Load Transient Response
- Up to 700mA Load Current
- Low Quiescent Current (one Channel) : 200μA
- Output Voltage: 0.6V ~ 5.5V
- Automatic PWM/PFM Mode Switching
- No Schottky Diode Required
- 1.4MHz Constant Frequency Operation
- Short-Circuit Protection
- Shutdown Quiescent Current: < 1μA
- DFN3*3-10L Package

Applications

- Digital cameras and MP3
- Palmtop computers / PDAs
- Cellular phones
- Wireless handsets and DSL modems
- PC cards

Description

The JTMH1006 is a high efficiency synchronous, dual channel PWM step-down DC/DC converter working under an input voltage range from 2.5V to 5.5V. It integrates two PWM synchronous step-down DC-DC converters. 100% duty cycle capability extends battery life in portable devices, while the quiescent current (one channel) is 200μA with no load, and drops to <1μA in shutdown.

Each DC-DC converter has independent enable input and short-circuit protection allowing versatile power sequence combination.

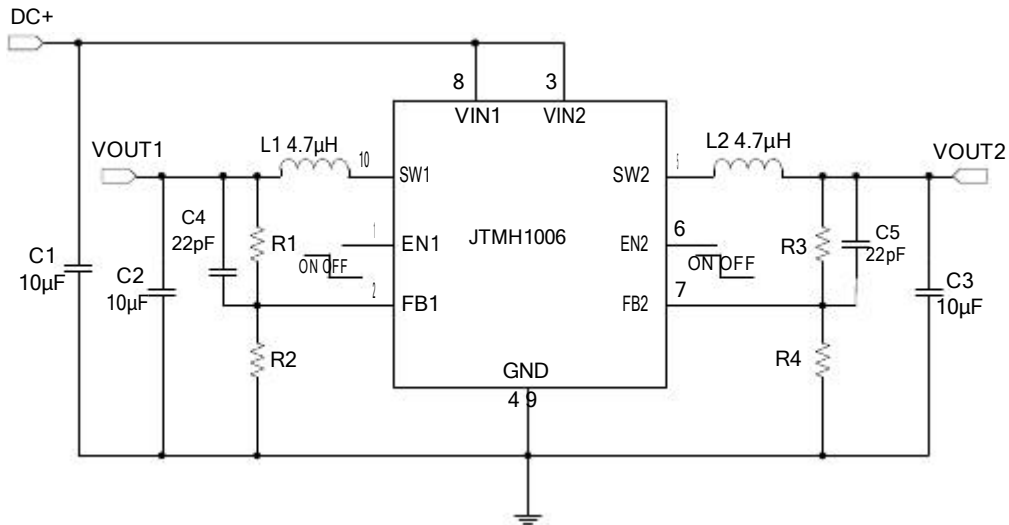
The JTMH1006 converters are available in the industry standard DFN3*3-10L packages (or upon request).

Order Information

JTMH1006- ① ② ③ ④:

Symbol	Description
①	Denotes Output Voltage: A: Adjustable Output
②	Denotes Package Types: J: DFN3*3-10L
③ ④	Internal Definition

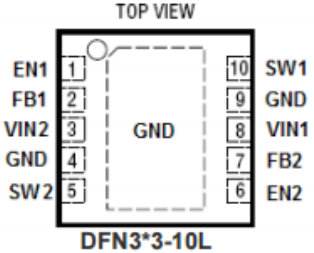
Typical Application Circuit



$$*V_{OUT1} = 0.6V \cdot [1 + (R1/R2)], V_{OUT2} = 0.6V \cdot [1 + (R3/R4)].$$

Model	VOUT (V)	VIN (V)	Package
JTMH1006-AJSC	0.6 ~ 5.5	2.5 ~ 5.5	DFN3*3-10L

Pin Assignment and Description

	PIN	NAME	DESCRIPTION
	1	EN1	ON/OFF Control 1(High Enable)
	2	FB1	Output Feedback 1
	3	VIN2	Input 2
	4,9	GND	Ground
	5	SW2	Switch Output 2
	6	EN2	ON/OFF Control 2(High Enable)
	7	FB2	Output Feedback 2
	8	VIN1	Input 1
	10	SW1	Switch Output 1

Absolute Maximum Ratings (Note 1)

- Power Dissipation.....Internally limited
- Supply Input Voltage,VIN1,VIN2.....-0.3V ~ 6V
- Output Voltage, VOUT1,VOUT2.....-0.3V ~ 6V
- EN1, EN2 Pin Voltage.....-0.3V ~ (VIN+0.3)V
- SW1, SW2 Pin Voltage.....-0.3V ~ (VIN+0.3)V
- SW1,SW2 Pin Current.....1.3A
- Operating Temperature Range(Note 2)-40°C ~ + 85°C
- Storage Temperature Range-65°C ~ + 150°C
- Junction Temperature-40°C ~ +125°C
- Lead Temperature (Soldering 10 sec.)+ 265°C

Note 1: Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

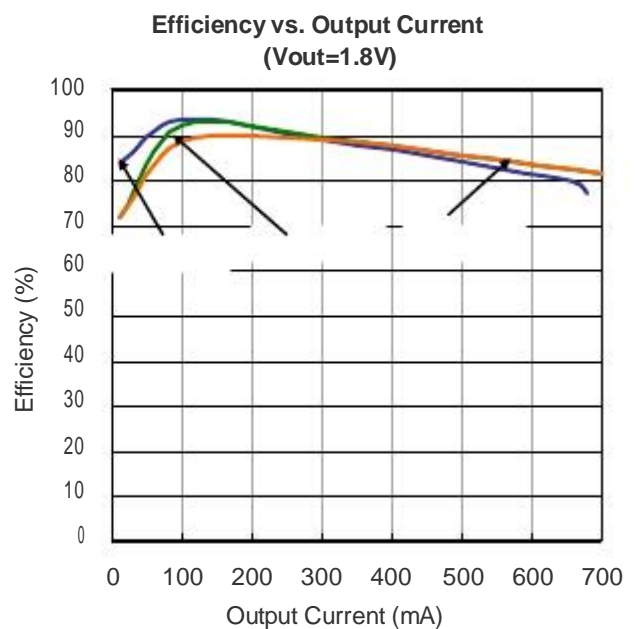
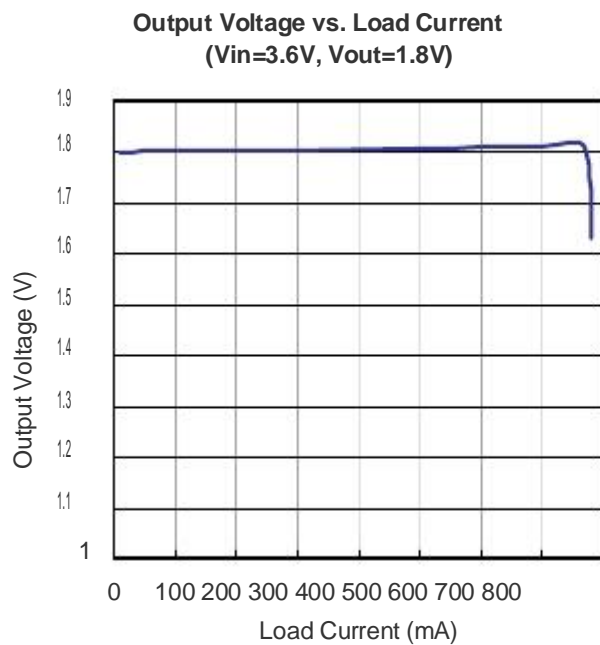
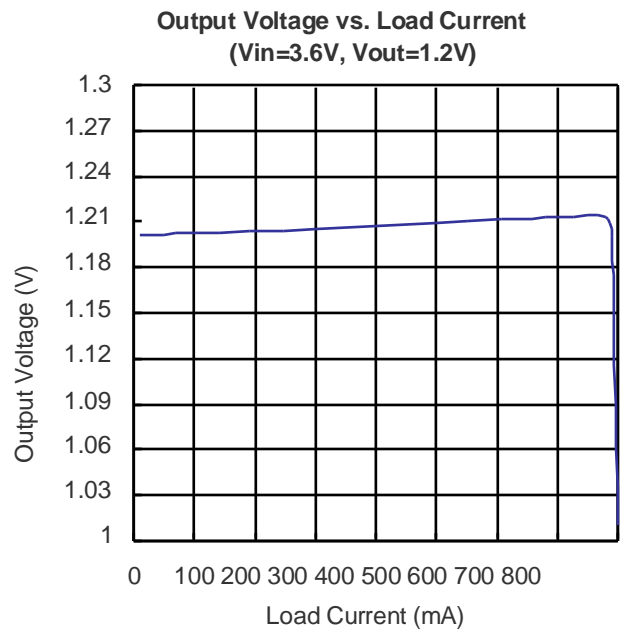
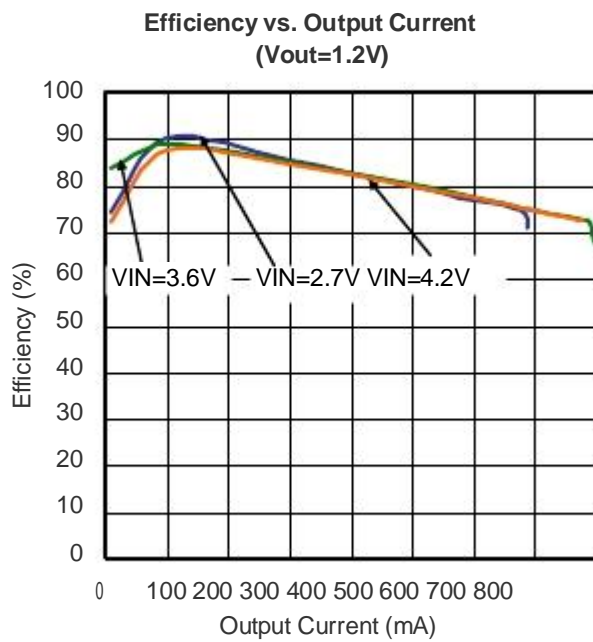
Note 2: The JTMH1006 is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Electrical Characteristics (VOUT1 or VOUT2)

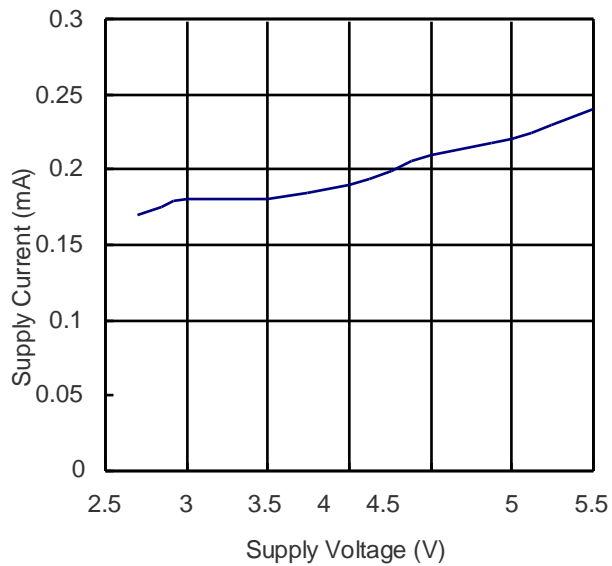
Operating Conditions: $T_A=25^{\circ}\text{C}$, $V_{IN}=3.6\text{V}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{OUT}	Output Voltage	I _{OUT} = 100mA, R1/R2=2	1.75	1.80	1.85	V
V _{IN}	Operating Voltage Range		2.5		5.5	V
V _{FB}	Regulated Voltage	T _A = 25°C	0.588	0.6	0.612	V
I _{FB}	Feedback Current				±30	nA
ΔV _{FB}	V _{REF}	V _{IN} =2.5V ~ 5.5V		0.03	0.4	%/V
f _{OSC}	Oscillator Frequency	V _{FB} = 0.6V or V _{OUT} = 100%		1.4		MHz
I _Q	Quiescent Current	V _{FB} = 0.5V or V _{OUT} = 90%, I _{LOAD} = 0A		200	300	μA
I _{SHDN}	Shutdown Current	V _{EN} = 0V, V _{IN} = 4.2V		0.1	1	μA
I _{PK}	Peak Inductor Current	V _{IN} = 3V, V _{FB} = 0.5V or V _{OUT} = 90%, Duty Cycle < 35%	0.8	0.95	1.1	A
R _{PFET}	R _{DS(ON)} of P-Channel FET	I _{SW} = 100mA		0.3		Ω
R _{NFET}	R _{DS(ON)} of N-Channel FET	I _{SW} = -100mA		0.39		Ω
ΔV _{LINE}	V _{OUT} Line Regulation	V _{IN} =2.5V ~ 5.5V		0.03	0.3	%/V
ΔV _{LOAD}	V _{OUT} Load Regulation			0.33		%
EFFI	Efficiency	When connected to ext. components V _{IN} =V _{EN} =2.7V, V _{OUT} =2.5V, I _{OUT} =100mA		95		%

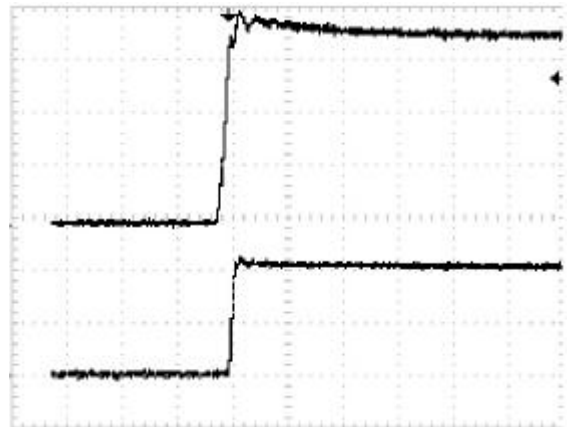
Typical Performance Characteristics (VOUT1 or VOUT2)



Supply Current vs. Supply Voltage
($V_{OUT}=1.8V$ $I_O=0A$)

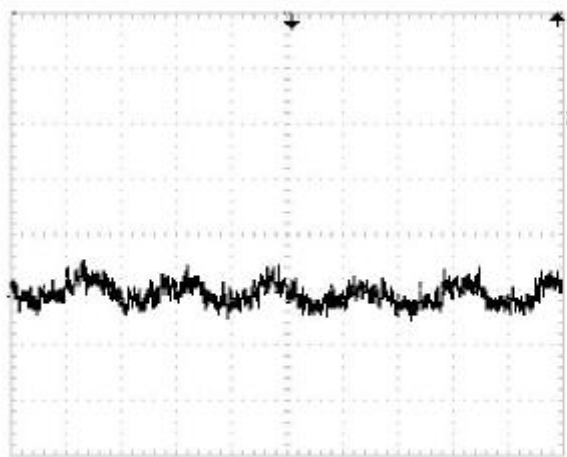


Start-up from Shutdown
(1.00V/div 1.00V/div 100 μ s/div)



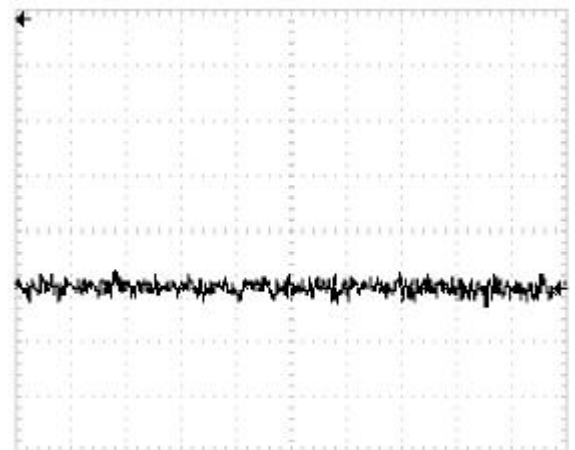
$V_{IN}=3.6V$ $V_{OUT}=1.8V$ $I_{LOAD}=0mA$

**Output Noise (10mV/DIV 200ns/DIV
AC COUPLED)**



$V_{IN}=3.6V$ $V_{OUT}=1.8V$ $I_{LOAD}=200mA$

**Output Noise (100mV/DIV 2ms/DIV
AC COUPLED)**



$V_{IN}=3.6V$ $V_{OUT}=1.8V$ $I_{LOAD}=0mA$

Pin Functions

EN1 (Pin 1): En Control Input. Forcing this pin above 1.3V enables the VOUT1. Forcing this pin below 0.7V can shut down the VOUT1. In shutdown, all functions are disabled drawing <1μA supply current. Do not leave EN1 floating.

FB1 (Pin 2): Output Feedback 1. Receive the feedback voltage from an external resistive divider across the output 1. The output voltage is set by a resistive divider according to the following formula: $V_{OUT1} = 0.6V \cdot [1 + (R1/R2)]$.

VIN2 (Pin 3): Supply Pin for VOUT2. It must be closely decoupled to GND, with a 10μF or greater ceramic capacitor.

GND (Pin 4, 9, 11): Ground Pin.

SW2 (Pin 5): Switch Node for VOUT2 Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

EN2 (Pin 6): En Control Input. Forcing this pin above 1.3V enables the VOUT2. Forcing this pin below 0.7V can shut down the VOUT2. In shutdown, all functions are disabled drawing <1μA supply current. Do not leave EN2 floating.

FB2 (Pin 7): Output Feedback 2. Receive the feedback voltage from the external resistive divider across the output. The output voltage is set by a resistive divider according to the following formula: $V_{OUT2} = 0.6V \cdot [1 + (R3/R4)]$.

VIN1 (Pin 8): Supply Pin for VOUT1. It must be closely decoupled to GND, with a 10μF or greater ceramic capacitor.

SW1 (Pin 10): Switch Node for VOUT1 Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

Application Information

The basic JTMH1006 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT} .

Inductor Selection

For most applications, the value of the inductor will fall in the range of $1\mu\text{H}$ to $4.7\mu\text{H}$. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in equation. A reasonable starting point for setting ripple current is $I_L = 320\text{mA}$ (40% of 800mA).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 960mA rated inductor should be enough for most applications ($800\text{mA} + 160\text{mA}$). For better efficiency, choose a low DC-resistance inductor.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or perm alloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field/EMI requirements than on what the JTMH1006 requires to operate.

Output and Input Capacitor Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN} . To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \approx I_{O\text{MAX}} \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left(\text{ESR} + \frac{1}{8fC_{OUT}} \right)$$

Where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume. Other capacitor types include Sanyo POSCAP, Kemet T510 and T495 series, and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as: $\text{Efficiency} = 100\% - (L1 + L2 + L3 + \dots)$ where $L1$, $L2$, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: V_{IN} quiescent current and I_2R losses. The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents whereas the I_2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The V_{IN} quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge ΔQ moves from V_{IN} to ground. The resulting $\Delta Q/t$ is the current out of V_{IN} that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$ where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

2. I_2R losses are calculated from the resistances of the internal switches, R_{SW} and external inductor R_L . In continuous mode the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows: $R_{SW} = R_{DS(ON)TOP} \times DC + R_{DS(ON)BOT} \times (1-DC)$ The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I_2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current. Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

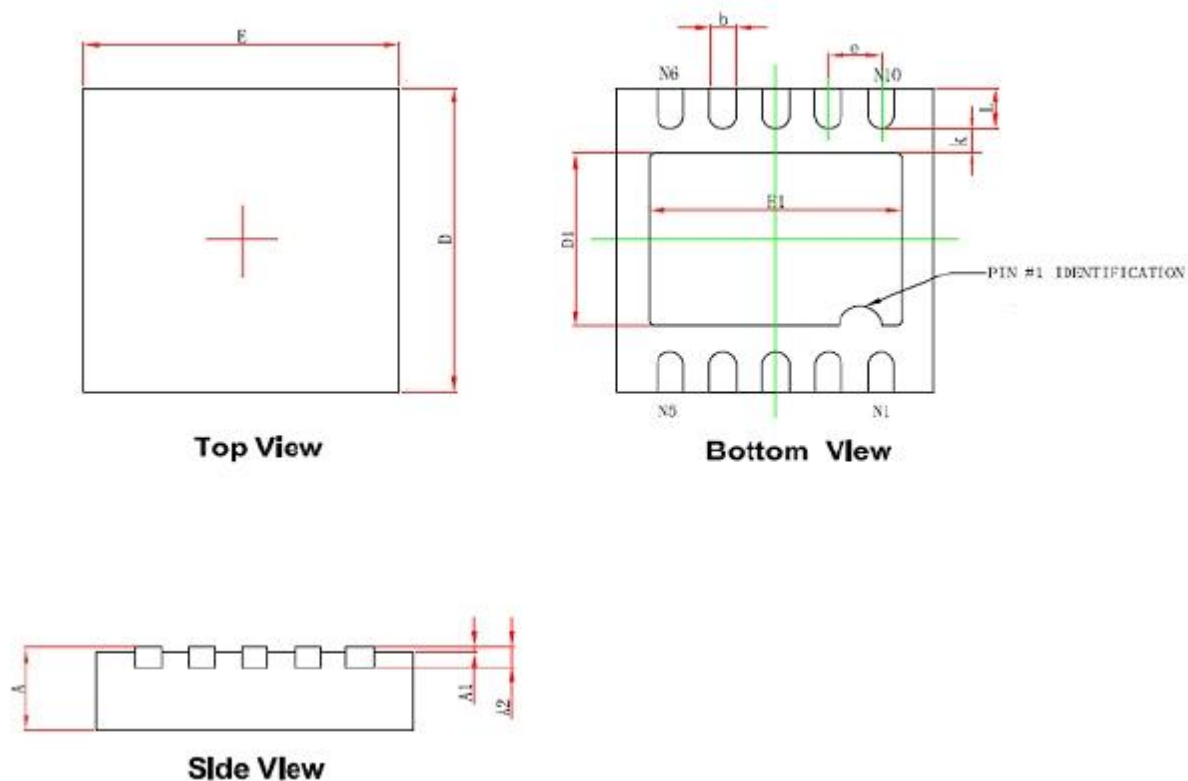
PCB Layout Guidelines

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the JTMH1006. Check the following in your layout:

1. The power traces, consisting of the GND trace, the SW trace and the VIN trace should be kept short, direct and wide.
2. Put the input capacitor as close as possible to the device pins (VIN and GND).
3. SW node is with high frequency voltage swing and should be kept small area. Keep analog components away from SW node to prevent stray capacitive noise pick-up.
4. Connect all analog grounds to a common node and then connect the common node to the power ground behind the output capacitors.
5. Keep the (–) plates of C_{IN} and C_{OUT} as close as possible.

Packaging Information

DFN3*3-10L Package Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A2	0.153	0.253	0.006	0.010
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E1	2.300	2.500	0.091	0.098
k	0.200MIN		0.008MIN	
b	0.200	0.300	0.008	0.012
e	0.500TYP		0.020TYP	
L	0.300	0.500	0.012	0.020