Synchronous Buck DC/DC Converter

Features

- Up to 93% Efficiency
- Low Quiescent Current: 200μA
- Up to 1.4A Load Current
- Input Voltage: 2.5V ～ 5.5V
- No Schottky Diode Required
- 950kHz Fixed Frequency Switching
- 0.8V Reference Allows Low Output Voltages
- Short-Circuit Protection
- Shutdown Quiescent Current: <1μA
- SOT-23-5L Package (lead-free package)

Applications

- Digital Cameras and MP3
- Palmtop Computers / PDAs
- Cellular Phones
- Wireless Handsets and DSL Modems
- PC Cards
- Portable Media Players

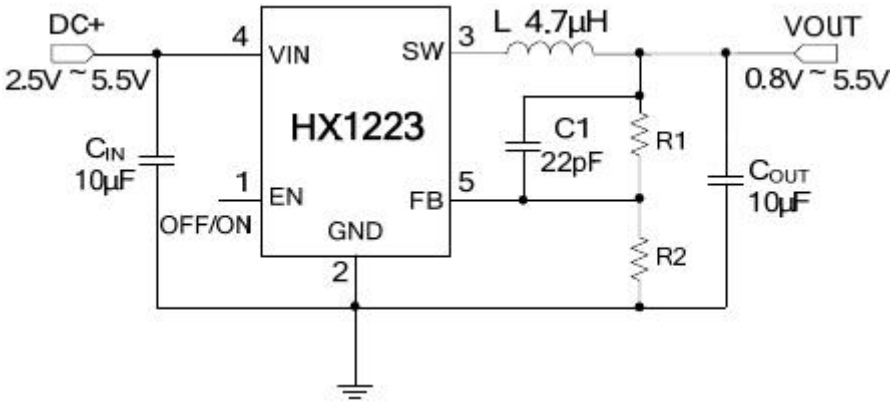
Description

The JTMH1223 is a high efficiency synchronous, buck DC/DC converter using a constant frequency, current mode architecture. 100% duty cycle capability extends battery life in portable devices, while the supply current is 200μA with no load, and drops to <1μA in shutdown. The 2.5V to 5.5V input voltage range makes the JTMH1223 ideally suited for single Li-Ion battery-powered applications.

Switching frequency is internally set at 0.95MHz, allowing the use of small surface mount inductors and capacitors.

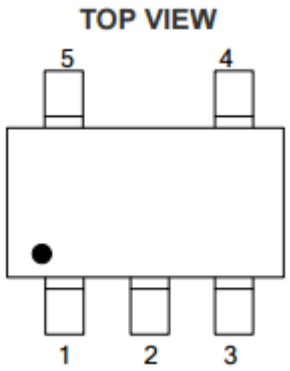
The internal synchronous switch increases efficiency and eliminates the need for an external Schottky diode. Low output voltages are easily supported with the 0.8V feedback reference voltage. The JTMH1223 is available in a low profile SOT-23-5L package.

Typical Application Circuit



* The output voltage is adjustable: $V_{OUT} = 0.8V \cdot [1 + (R1/R2)]$

Pin Assignment and Description



PIN	NAME	DESCRIPTION
1	EN	ON/OFF Control (High Enable)
2	GND	Ground
3	SW	Switching node for Output
4	VIN	Power Input
5	FB	Feedback Pin

Absolute Maximum Ratings (Note 1)

- Input Supply Voltage .....–0.3V ～ 6V
- EN, FB Voltages ..... –0.3V ～ VIN
- SW Voltage ..... –0.3V ～ (VIN + 0.3V)
- Peak SW Sink and Source Current..... 3A
- Operating Temperature Range (Note 2).....–40℃ ～ +85℃
- Storage Temperature Range.....–65℃ ～ +150℃
- Lead Temperature (Soldering, 10 sec).....+265℃
- Junction Temperature Range……–40℃ ～ +125℃
- Power Dissipation, PD @ TA = 25°C ……..…0.346W

ESD Susceptibility

- HBM (Human Body Mode) ……..2KV
- MM (Machine Mode) ……. 50V

Note 1: Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability

Note 2: The JTMH1223 is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

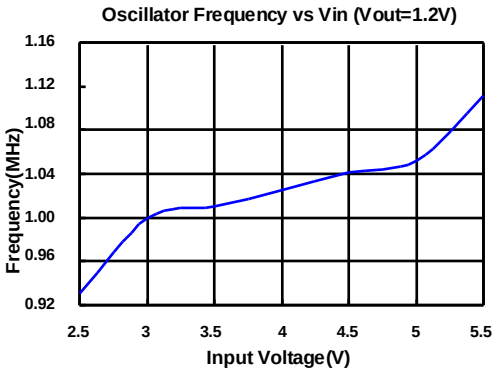
Electrical Characteristics

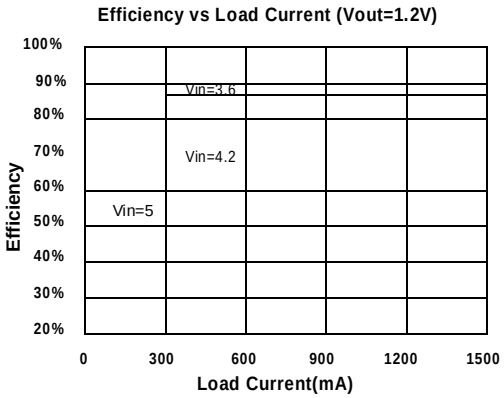
Operating Conditions: TA=25℃, V_{IN}=5V, unless otherwise specified.

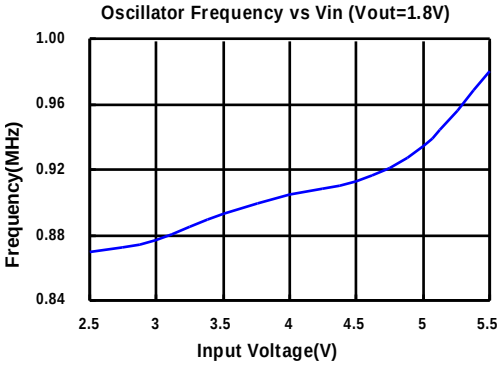
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Operating Voltage Range		2.5		5.5	V
V_{FB}	Regulated Voltage	TA = 25℃	0.78	0.8	0.82	V
f_{OSC}	Oscillator Frequency	V_{FB} = 0.8V or V_{OUT} = 100%		0.95		MHz
I_Q	Quiescent Current	I_{LOAD} = 0A		200		μA
I_{SHDN}	Shutdown Current	V_{EN} = 0V		0.1		μA
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET	I_{SW} = 300mA		0.2		Ω
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET	I_{SW} = -300mA		0.27		Ω
V_{ENL}	EN Falling Threshold				0.4	V
V_{ENH}	En Rising Threshold		1.5			V
ΔV_{UVLO}	UVLO Hysteresis			0.1		V
V_{UVLO}	Input UVLO Threshold			1.6		V
EFFI	Efficiency	When connected to ext. components V_{IN}=4.2V,V_{OUT}=3.3V, I_{OUT}=300mA		93		%
T_{SD}	Thermal Shutdown Temperature			160		℃
DC	Max Duty Cycle		100			%

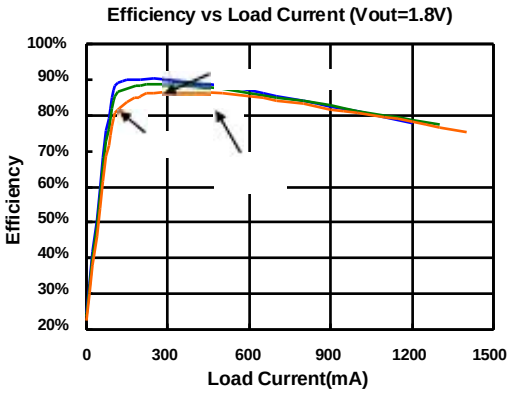
Typical Performance Characteristics

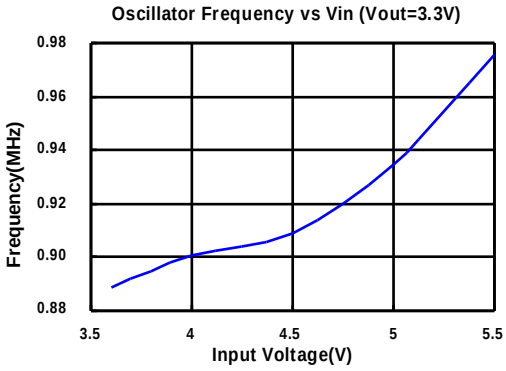
Operating Conditions: TA=25℃, CIN =10μF, COUT =10μF, L=4.7μH, unless otherwise noted.

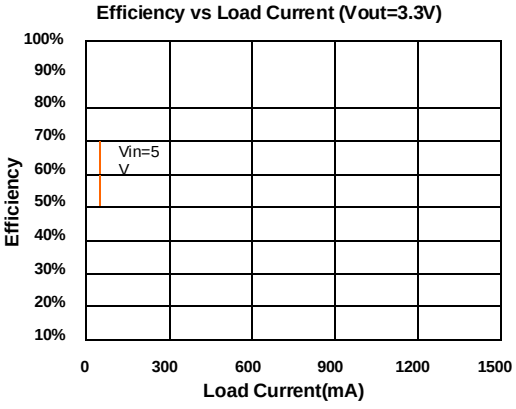




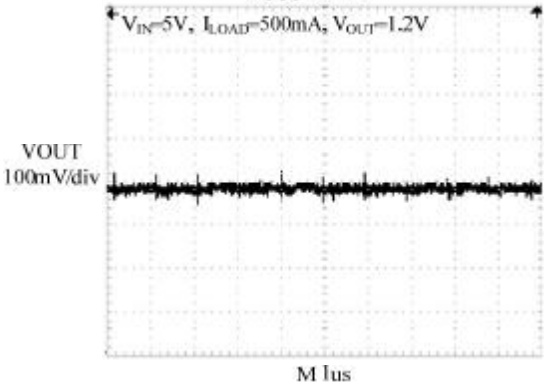




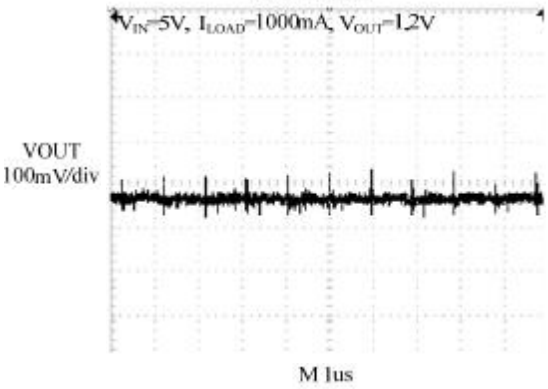




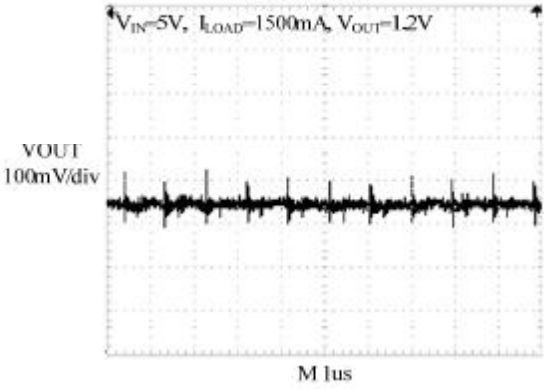
V_{OUT} Noise



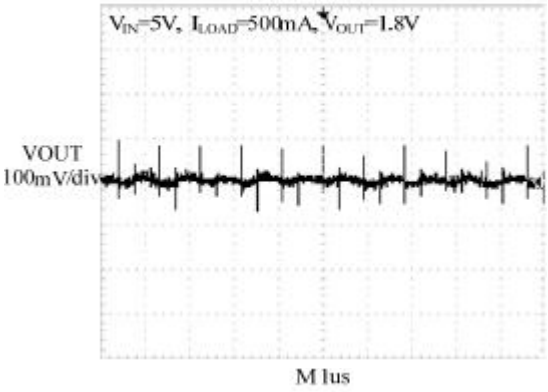
V_{OUT} Noise



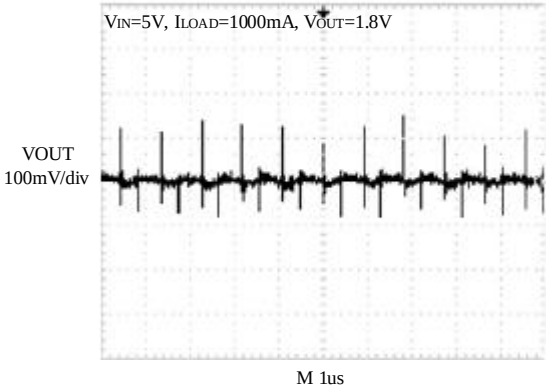
V_{OUT} Noise



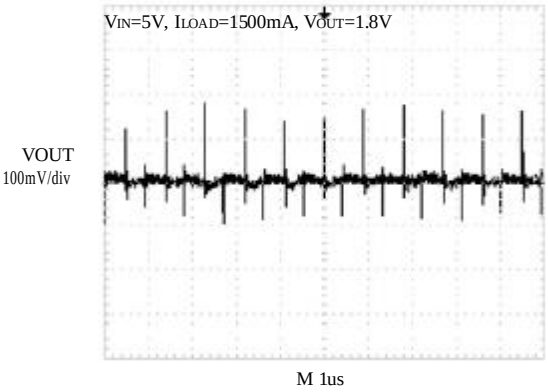
V_{OUT} Noise

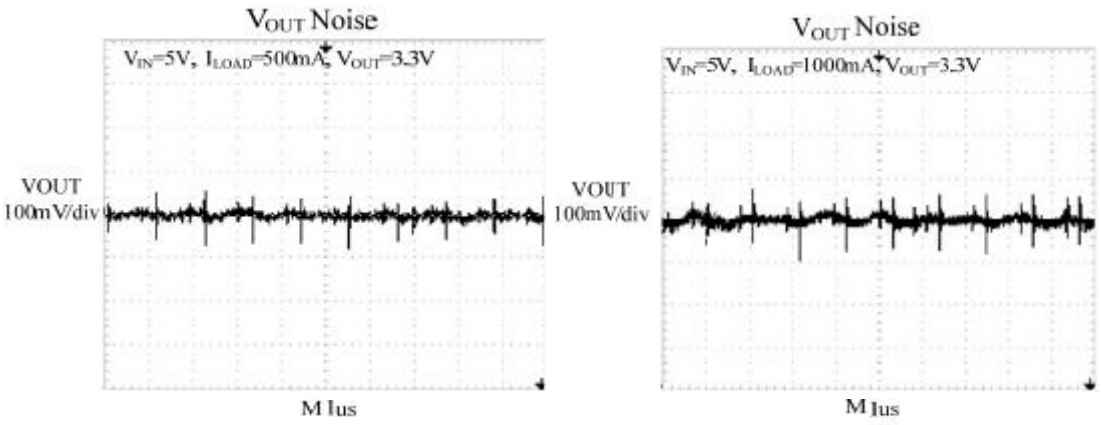


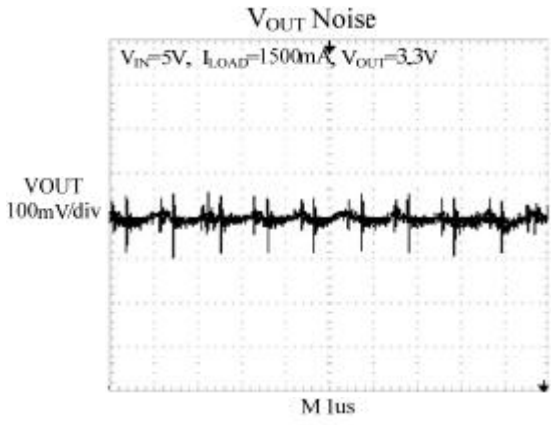
V_{OUT} Noise

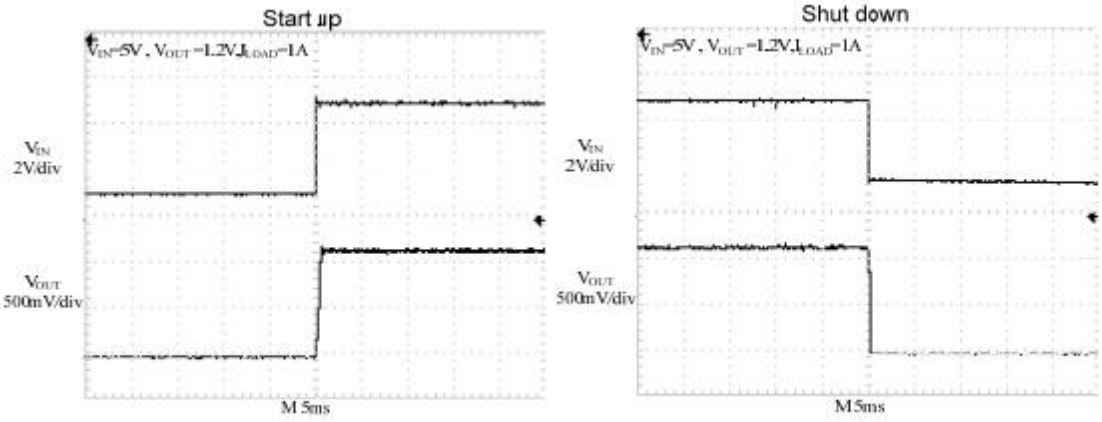


V_{OUT} Noise

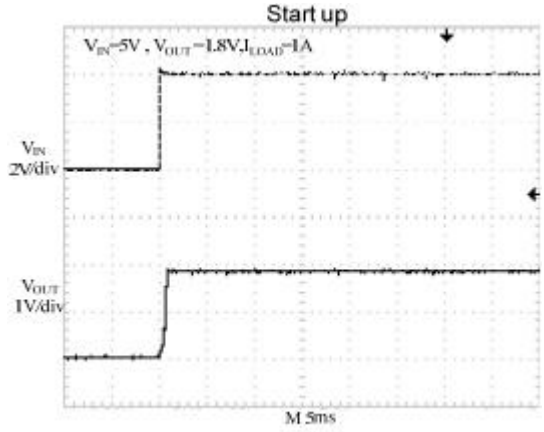



VOUT Noise
VIN=5V, ILOAD=500mA, VOUT=3.3V
VOUT
100mV/div
M 1us
VOUT Noise
VIN=5V, ILOAD=1000mA, VOUT=3.3V
VOUT
100mV/div
M 1us

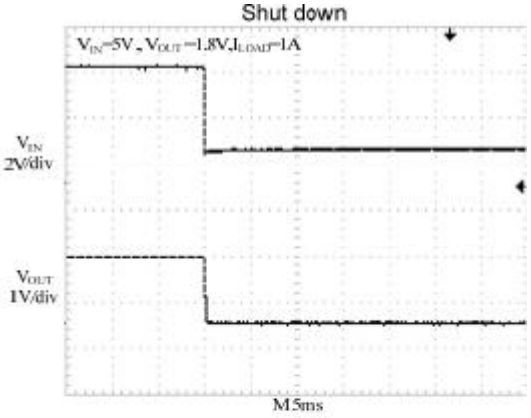

VOUT Noise
VIN=5V, ILOAD=1500mA, VOUT=3.3V
VOUT
100mV/div
M 1us


Start up
VIN=5V, VOUT=1.2V, ILOAD=1A
VIN
2V/div
VOUT
500mV/div
M 5ms
Shut down
VIN=5V, VOUT=1.2V, ILOAD=1A
VIN
2V/div
VOUT
500mV/div
M 5ms

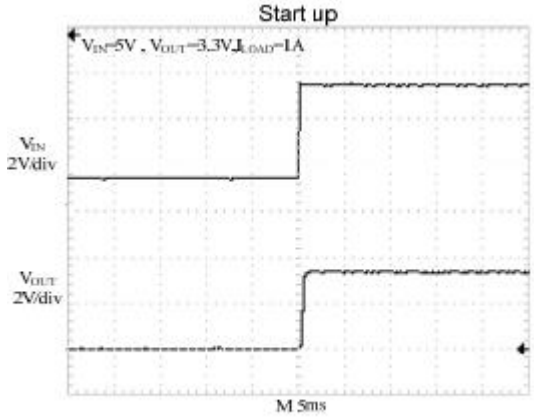
Start up



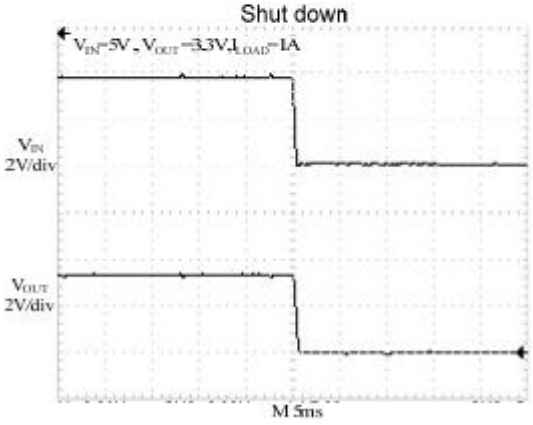
Shut down



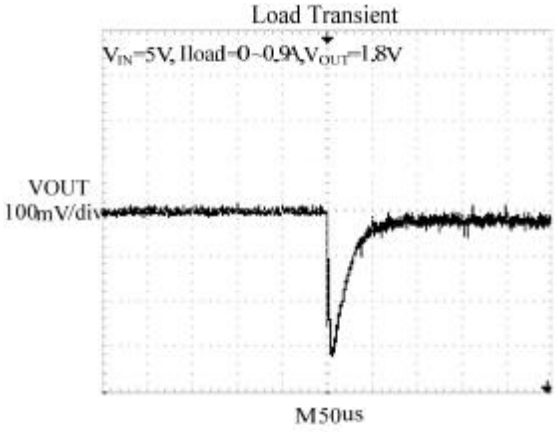
Start up



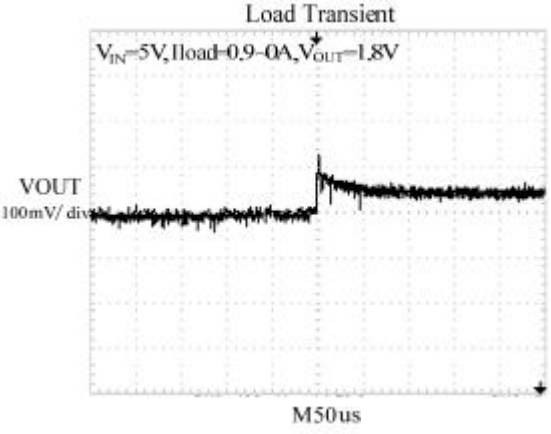
Shut down



Load Transient



Load Transient



Pin Description

EN (Pin 1): En Control Input. Forcing this pin above 1.5V enables the part. Force this pin below 0.4V shutdown the device. In shutdown, all functions are disabled drawing <1μA supply current. Do not leave EN floating.

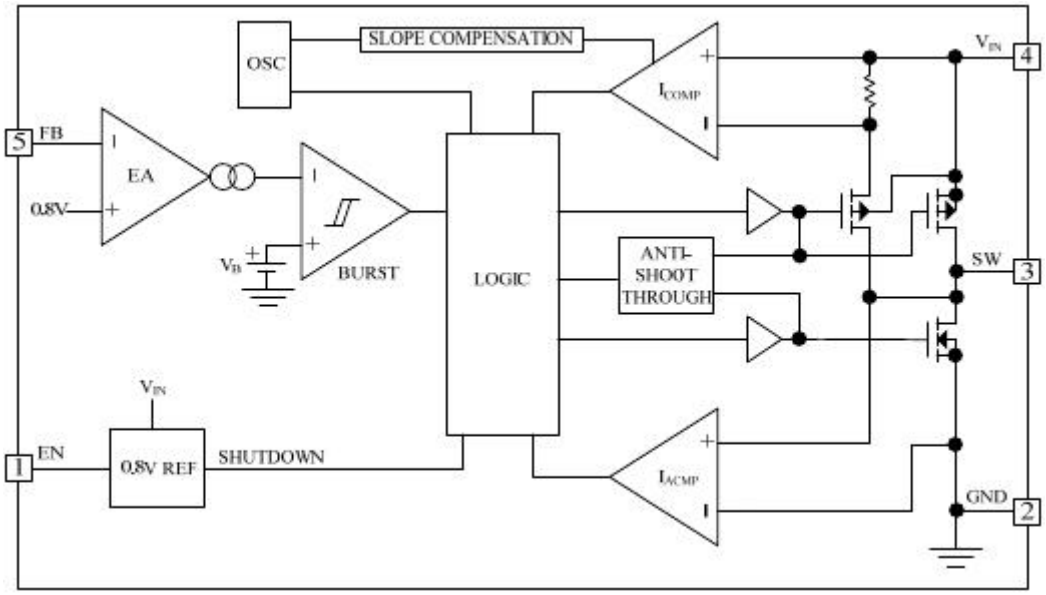
GND (Pin 2): Ground Pin.

SW (Pin 3): Switch Node Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

VIN (Pin 4): Main Supply Pin. Must be closely decoupled to GND, Pin2，with a ceramic capacitor.

FB (Pin 5): Feedback Pin. Receive the feedback voltage from an external resistive divider across the output. The output voltage is set by a resistive divider according to the following formula: V_{OUT} = 0.8V · [1 + (R1/R2)].

Block Diagram



Application Information

Inductor Selection

For most applications, the value of the inductor will fall in the range of 4.7μH to 10μH. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in equation . A reasonable starting point for setting ripple current is I_L = 560mA (40% of 1.4A).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 1.68A rated inductor should be enough for most applications (1.4A + 280mA). For better efficiency, choose a low DC-resistance inductor.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or perm alloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field/EMI requirements than on what the JTMH1223 requires to operate.

Output and Input Capacitor Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \simeq I_{OMAX} \frac{\left[V_{OUT}(V_{IN} - V_{OUT})\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR).Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \simeq \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}}\right)$$

Where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as: Efficiency = 100% - (L1+ L2+ L3+ ...) where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: VIN quiescent current and I^2R losses. The VIN quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The VIN quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge Q moves from VIN to ground. The resulting Q/t is the current out of VIN that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f (Q_T+Q_B)$ where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to VIN and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW} and external inductor R_L. In continuous mode the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows: $R_{SW} = R_{DS(ON)TOP} \times DC + R_{DS(ON)BOT} \times (1-DC)$ The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current. Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

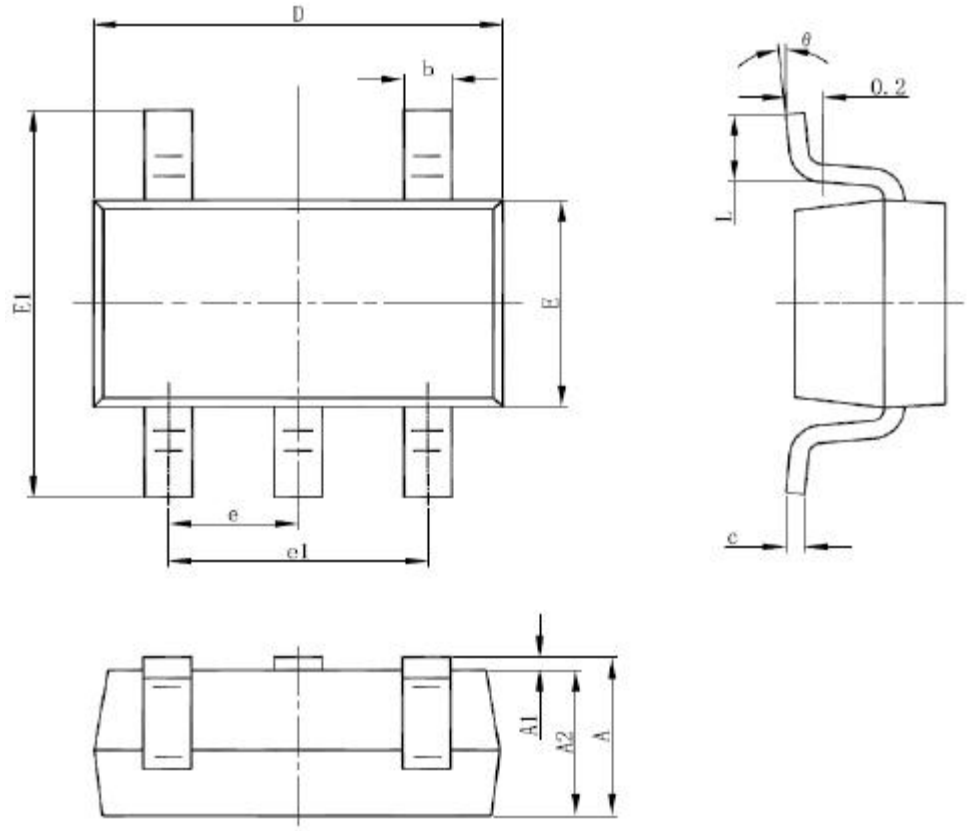
Board Layout Suggestions

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the JTMH1223. Check the following in your layout.

1. The power traces, consisting of the GND trace, the SW trace and the VIN trace should be kept short, direct and wide.
2. Put the input capacitor as close as possible to the device pins (VIN and GND).
3. SW node is with high frequency voltage swing and should be kept small area. Keep analog components away from SW node to prevent stray capacitive noise pick-up.
4. Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.

Packaging Information

SOT-23-5L Package Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°