Two Channels Integrated Power Management IC for Handheld Portable Equipment

Features

- Integrated Synchronous Boost Converter and USB Current-Limit Power Switch
- Low Quiescent Current: 230μA
- Wide Input Voltage Range: 2V to 5V
- USB Current Limiting at 1.4A
- Auxiliary Output VOUT1: 3V to 5.5V
- Efficiency up to 90%
- MSOP-10L Package

Applications

- Battery-Powered Equipment
- Motherboard USB Power Switch
- Hot-Plug Power Supplies
- Battery-Charger Circuits
- USB Device Power Switch
- DSC
- LCD Panel
- Wireless Equipment

Description

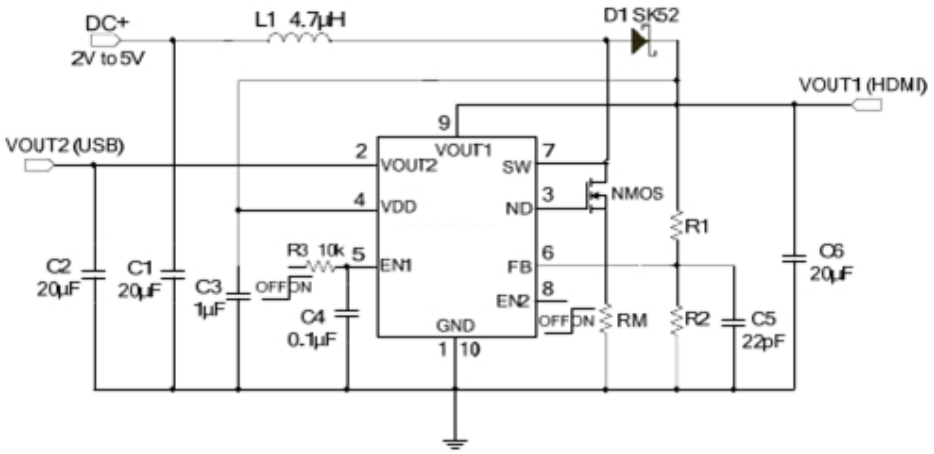
The JTMH7402 is an integrated USB power switch with boost converter to meet USB 5V power requirements from a 2V to 5V input supply. The features include a USB compliant power output, output switch enable, thermal shutdown and current limit.

The USB power switch is an integrated 200mΩ power switch with current limiting protection at 1.4A.

The boost converter output is an auxiliary 3V to 5.5V output to power additional loads. Its Load current can program by an external resistor from as low as 130mA to as high as 2000mA. It can operate in stable waveforms without external compensation.

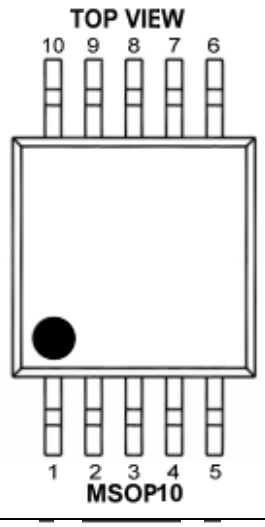
The JTMH7402 is available in tiny 10-Pin MSOP Package.

Typical Application Circuit



*V_{OUT1} = 1.212V · [1 + (R1/R2)], V_{OUT2} = V_{OUT1}. The resistor RM can be set to 50mΩ usually.

Pin Assignment and Description



PIN	NAME	DESCRIPTION
1,10	GND	Ground
2	VOUT2	Output Pin 2
3	ND	NMOS Drive
4	VDD	Input
5	EN1	ON/OFF Control for VOUT1 (High Enable)
6	FB	Feedback Pin for VOUT1
7	SW	Switch Output
8	EN2	ON/OFF Control for VOUT2 (High Enable)
9	VOUT1	Output Pin 1

Absolute Maximum Ratings (Note 1)

- Supply Voltage……−0.3V ～ 6V
- SW Pin Switch Voltage……−0.3V ～ 28V
- Other I/O Pin Voltages……−0.3V ～ 6V
- SW Pin Switch Current ……3A
- Operating Temperature(Note 2)……-40℃ ～ +85℃
- Operating Junction Temperature……-40℃ ～ +125℃
- Storage Temperature Range ……−65℃ ～ +150℃
- Lead Temperature……+265℃

Note 1: Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: The JTMH7402 is guaranteed to meet performance specifications from 0℃ to 70℃. Specifications over the –40℃ to 85℃ operating temperature range are assured by design, characterization and correlation with statistical process controls.

Electrical Characteristics

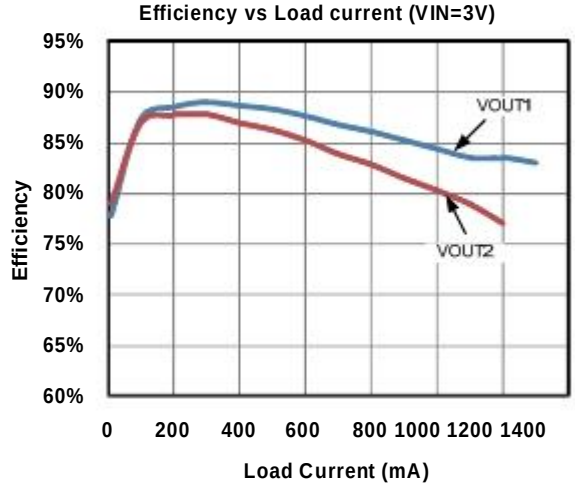
Operating Conditions: TA=25°C, C1=C2=C6=20μF, L1=4.7μH, C3=1μF, C4=0.1μF, C5=22pF, R1=75kΩ, R2=22.7KΩ, R3=10kΩ, D1=SK52, NMOS=2302, RM=50mΩ, unless otherwise noted.

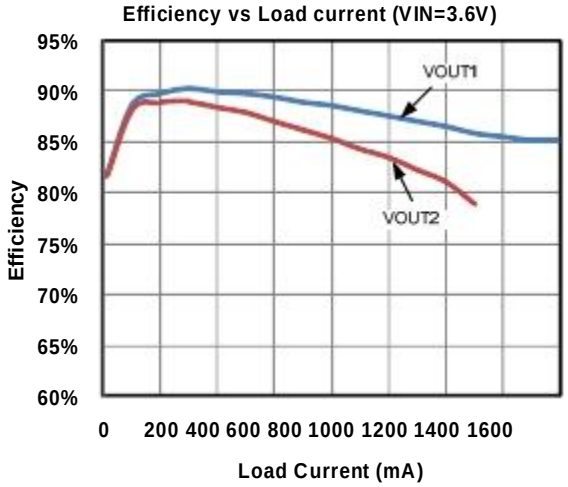
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{START}	Start-up Voltage	I_{LOAD}=1mA		1.5		V
V_{IN}	Input Voltage Range		2		5	V
V_{OUT1}	VOUT1 Adjust Range		3		5.5	V
V_{OUT2}	VOUT2 Adjust Range	V_{OUT2}=V_{OUT1}				
I_Q	No Load Quiescent Supply Current I (V_{IN})	V_{IN}=3.6V		230		μA
I_{SHDN}	Shutdown Supply Current	EN1=EN2="0"		30		μA
V_{FB}	Feedback Reference Voltage			1.17		V
R_{NFET}	NMOS SW ON Resistance (VOUT1)	V_{IN}=3.6V, V_{OUT1}=5V, I_{OUT1} = 500mA		50		mΩ
I_{LIM1-N}	NMOS Current Limit (VOUT1)			3		A
V_{EN1}	En1 Input High(Start up)	V_{IN}=3.6V, V_{OUT1}=5V	1.5			V
I_{LIM2}	Current Limit Threshold (VOUT2)			1.4		A
V_{EN2H}	En2 Input High(Start up)	V_{IN}=3.6V, V_{OUT2}=5V	1.5			V
V_{EN2L}	En2 Input Low(Shut down)	V_{IN}=3.6V, V_{OUT2}=5V			0.4	V
ΔV_{LOAD}	Load Regulation	V_{IN}=3.6V, I_{LOAD}=1mA ～ 1A		0.17		mV/mA
$R_{DS(ON)}$	Output NMOFET	V_{IN}=5V, I_{OUT2}=500mA		200		mΩ
EFFI	Efficiency	V_{IN}=3.6V, V_{OUT1}=5V, I_{OUT1}=500mA		87		%

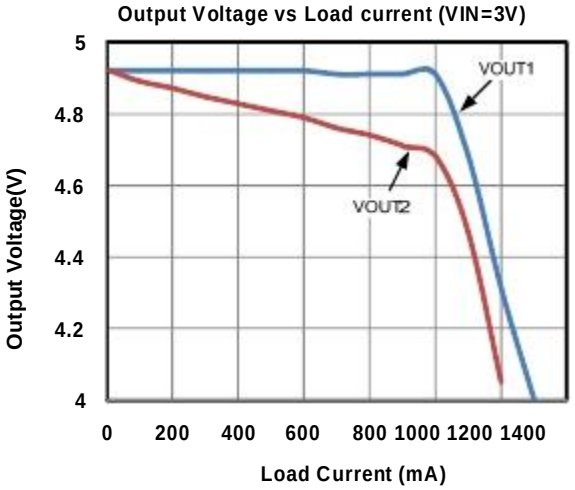
*EFFI = [(Output Voltage × Output Current) / (Input Voltage × Input Current)] × 100%

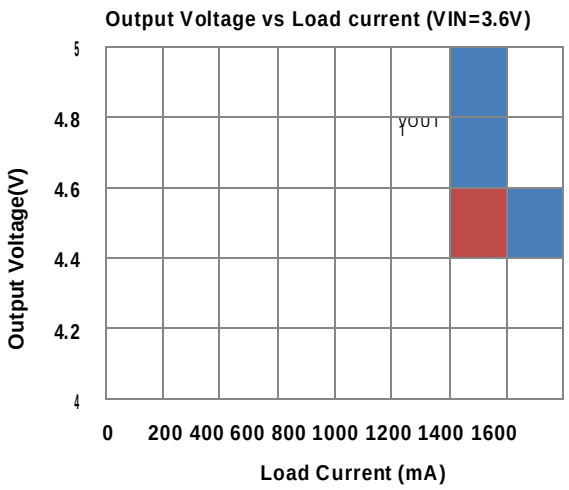
Typical Performance Characteristics

Operating Conditions: T_A=25℃, C1=C2=C6=20μF, L1=4.7μH, C3=1μF, C4=0.1μF, C5=22pF, R1=75kΩ, R2=22.7kΩ, R3=10kΩ, D1=SK52, NMOS=2302, RM=50mΩ, unless otherwise noted.









Pin Functions

GND (Pin 1, 10): Signal and Power Ground. Provide a short direct PCB path between GND and the (–) side of the output capacitor(s).

VOUT2 (Pin 2): Connected to a USB. Bypass VOUT2 with ESR capacitor. However stability improves with higher ESRs.

ND (Pin 3): Drive of the N-Channel MOSFET. Connect to the Gate of N-Channel MOSFET.

VDD (Pin 4): Input positive power pin.

EN1 (Pin 5): Enable for VOUT1 (Active High). Pull this pin high to enable the VOUT1. Tie to GND to shut down the VOUT1. Never let this pin floating.

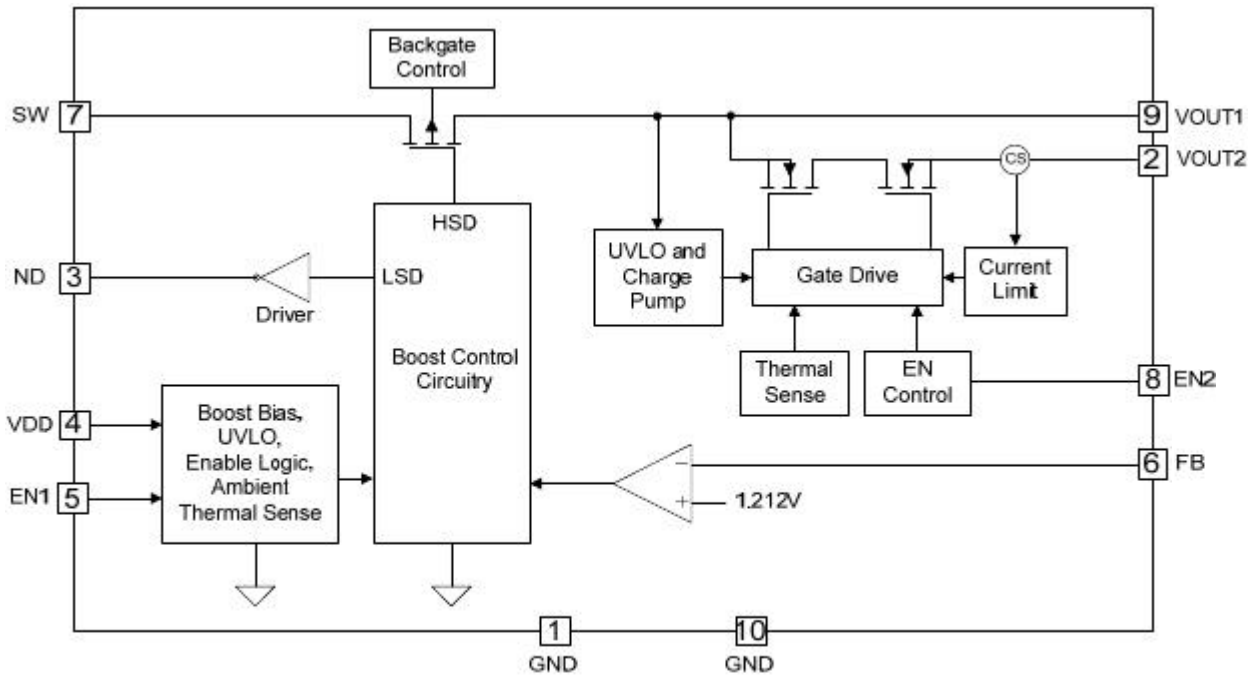
FB (Pin 6): Feedback Input to the g_m Error Amplifier. Connect resistor divider tap to this pin. The VOUT1 can be adjusted from 3V to 5.5V by: $V_{OUT1} = 1.212V \cdot [1 + (R1/R2)]$.

SW (Pin 7): Switch Pin. Connect inductor between SW and VIN. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot.

EN2 (Pin 8): Enable for VOUT2 (Active High). Pull this pin high to enable the VOUT2. Tie to GND to shut down the VOUT2. Do not leave EN floating.

VOUT1 (Pin 9): Connected to the HDMI. Bypass VOUT1 with ESR capacitor. However stability improves with higher ESRs.

Block Diagram



Application Information

Output and Input Capacitor Selection

Low ESR (equivalent series resistance) capacitors should be used to minimize the output voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have extremely low ESR and are available in small footprints. A 4.7μF to 20μF output capacitor is sufficient for most applications. Larger values up to 22μF may be used to obtain extremely low output voltage ripple and improve transient response. An additional phase lead capacitor may be required with output capacitors larger than 10μF to maintain acceptable phase margin. X5R and X7R dielectric materials are preferred for their ability to maintain capacitance over wide voltage and temperature ranges.

Low ESR input capacitors reduce input switching noise and reduce the peak current drawn from the battery. It follows that ceramic capacitors are also a good choice for input decoupling and should be located as close as possible to the device. A 20μF input capacitor is sufficient for virtually any application. Larger values may be used without limitations.

Output Voltage Setting (VOUT1)

Referring to Typical Application Circuits, the output voltage of the switching regulator (V_{OUT}) can be set with Equation (1).

$$V_{OUT1}=(1+\frac{R1}{R2}) \times 1.212V \quad (1)$$

Feedback Loop Design (VOUT1)

Referring to Typical Application Circuits, the selection of R1 and R2 based on the trade-off between quiescent current consumption and interference immunity is stated below:

- Follow Equation (1)
- Higher R reduces the quiescent current (Path current=1.212V/R2), however resistors beyond 5MW are not Recommended.
- Lower R gives better noise immunity, and is less sensitive to interference, layout parasitics, FB node leakage, and improper probing to FB pin.

For applications without standby or suspend modes, lower values of R1 and R2 are preferred. For applications concerning the current consumption in standby or suspend modes, the higher values of R1 and R2 are needed. Such high impedance feedback loop is sensitive to any interference, which requires careful PCB layout and avoid any interference, especially to FB pin. To improve the system stability, a proper value capacitor between FB pin and GND pin is suggested. An empirical suggestion is around 22pF.

Current Limiting and Short Protection (VOUT2)

The current limit circuit is designed to protect the system supply, the MOSFET switch and the load from damage caused by excessive currents. The current limit threshold is set internally to limits the output current to approximately 1.4A typical. When a heavy load or short circuit is applied to an enabled switch, a large transient current may flow until the current limit circuitry responds. Once this current limit threshold is exceeded the device enters constant current mode until the thermal shutdown occurs or the

fault is removed.

Filtering (VOUT2)

To limit the input voltage drop during hot-plug events connect a 10μF ceramic capacitor from V_{IN} to GND. However, higher capacitor values will further reduce the voltage drop at the input.

Connect a sufficient capacitor from VOUT to GND. This capacitor helps to prevent inductive parasitics from pulling VOUT2 negative during turn-off or EMI damage to other components during the hot detachment. It is also necessary for meeting the USB specification during hot plug-in operation. If VOUT2 is implanted in device end application, minimum 10μF capacitor from VOUT to GND is recommended and higher capacitor values are also preferred.

In choosing these capacitors, special attention must be paid to the Effective Series Resistance, ESR, of the capacitors to minimize the IR drop across the capacitor's ESR. A lower ESR on this capacitor can get a lower IR drop during the operation.

Ferrite beads in series with all power and ground lines are recommended to eliminate or significantly reduce EMI. In selecting a ferrite bead, the DC resistance of the wire used must be kept to a minimum to reduce the voltage drop.

Layout and Thermal Dissipation

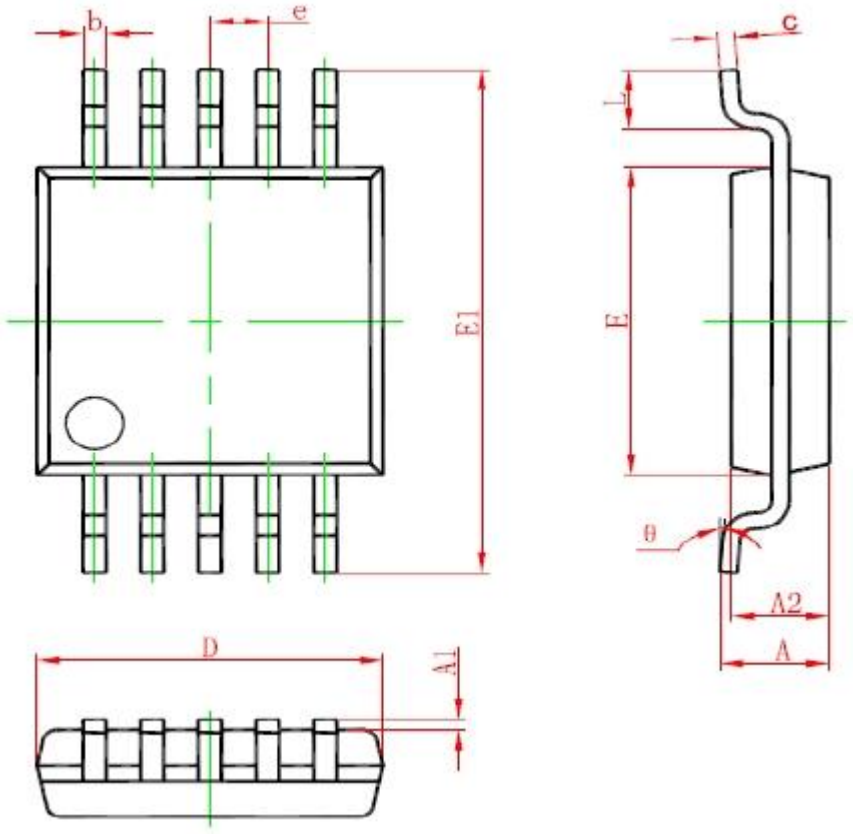
1. Place the switch as close to the USB connector as possible. Keep all traces as short as possible to reduce the effect of undesirable parasitic Inductance.

2. Place the output capacitor and ferrite beads as close to the USB connector as possible. If ferrite beads are used, use wires with minimum resistance and large solder pads to minimize connection resistance.

3. Under normal operating conditions, the package can dissipate the channel heat away. Wide power bus planes connected to VIN and VOUT and a ground plane in contact with the device will help dissipate additional heat.

Packaging Information

MSOP-10L Package Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
C	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.50(BSC)		0.020(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°