Inductor Built-in Step-Down “micro DC/DC” Converters

☆GreenOperation Compatible

■GENERAL DESCRIPTION

The JTMT201XCL/JTMT201XCL series is a synchronous step-down micro DC/DC converter which integrates an inductor and a control IC in one tiny package (2.5mm×2.0mm, h=1.0mm). A stable power supply with an output current of 400mA is configured using only two capacitors connected externally.

Operating voltage range is from 2.0V to 6.0V. Output voltage is internally set in a range from 0.8V to 4.0V in increments of 0.05V. The device is operated by 1.2MHz, and includes 0.42ΩP-channel driver transistor and 0.52ΩN-channel switching transistor. As for operation mode, the JTMT201XCL series is PWM control, the JTMT202XCL series is automatic PWM/PFM switching control, allowing fast response, low ripple and high efficiency over the full range of loads (from light load to heavy load). During stand-by, the device is shutdown to reduce current consumption to as low as 1.0μA or less. With the built-in UVLO (Under Voltage Lock Out) function, the internal driver transistor is forced OFF when input voltage becomes 1.4V or lower. The series provide short-time turn-on by the soft start function internally set in 0.25ms (TYP). The series integrate C_L auto discharge function which enables the electric charge stored at the output capacitor C_L to be discharged via the internal auto-discharge switch located between the L_X and V_{SS} pins. When the devices enter stand-by mode, output voltage quickly returns to the V_{SS} level as a result of this function.

■APPLICATIONS

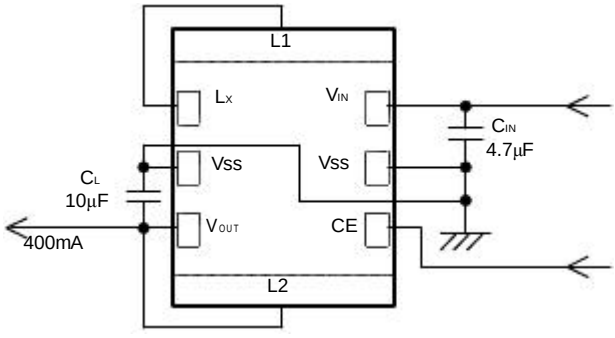
- ●Mobile phones, Smart phones
- ●Bluetooth Headsets
- ●WiMAX PDAs, MIDs, UMPCs
- ●Portable game consoles
- ●Digital cameras, Camcorders
- ●SSD(Solid State Drive)
- ●PND(Portable Navigation Device)

■FEATURES

Ultra Small	:	2.5mm×2.0mm, h=1.0mm
Input Voltage	:	2.0V ~ 6.0V
Output Voltage	:	0.8V ~ 4.0V (±2.0%)
High Efficiency	:	92%(V_{IN}=4.2V,V_{OUT}=3.3V)
Output Current	:	400mA
Oscillation Frequency	:	1.2MHz (±15%)
Maximum Duty Cycle	:	100%
Output Capacitor	:	Low ESR Ceramic
Function	:	Current Limiter Circuit (Constant Current & Latching) Soft-Start Circuit Built-In C_L Discharge
Control Methods	:	PWM (JTMT201) PWM/PFM Auto (JTMT202)
Operating Ambient Temperature	:	-40℃～+85℃
Environmentally Friendly	:	EU RoHS Compliant, Pb Free

■TYPICAL APPLICATION CIRCUIT

JTMT201XCL/JTMT202XCL Series

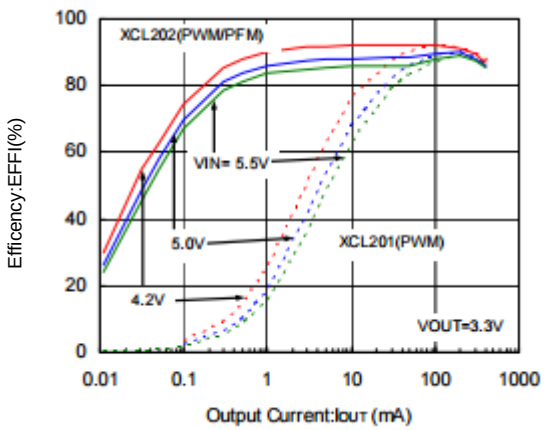


(TOP VIEW)

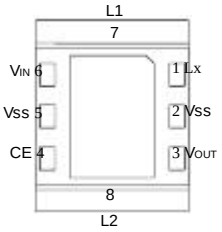
* “L1 and Lx”, and “L2 and VOUT” is connected by wiring.

■ TYPICAL PERFORMANCE CHARACTERISTICS

JTMT201XCLB331BR/JTMT202XCLB331BR



■PIN CONFIGURATION



(BOTTOM VIEW)

* It should be connected the VSS pin (No. 2 and 5) to the GND pin.
* If the dissipation pad needs to be connected to other pins, it should be connected to the GND pin.
* Please refer to pattern layout page for the connecting to PCB.

■PIN ASSIGNMENT

PIN NUMBER	PIN NAME	FUNCTIONS
1	L_X	Switching Output
2,5	V_{SS}	Ground
3	V_{OUT}	Output Voltage
4	CE	Chip Enable
6	V_{IN}	Power Input
7	L1	Inductor Electrodes
8	L2	

■PRODUCT CLASSIFICATION

•Ordering Information

JTMT201XCL①②③④⑤⑥-⑦(*1) Fixed PWM control

JTMT202XCL①②③④⑤⑥-⑦(*1) PWM / PFM automatic switching control

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Functions selection	B	C_L auto discharge, High speed soft-start
②③	Output Voltage	08～40	Output voltage options e.g. 1.2V → ②=1, ③=2 1.25V → ②=1, ③=C 0.05V increments : 0.05=A, 0.15=B, 0.25=C, 0.35=D, 0.45=E, 0.55=F, 0.65=H, 0.75=K, 0.85=L, 0.95=M
④	Oscillation Frequency	1	1.2MHz
⑤⑥-⑦	Package (Order Unit)	BR-G(*2)	CL-2025 (3,000pcs/Reel)
		ER-G(*3)	CL-2025-02 (3,000pcs/Reel)

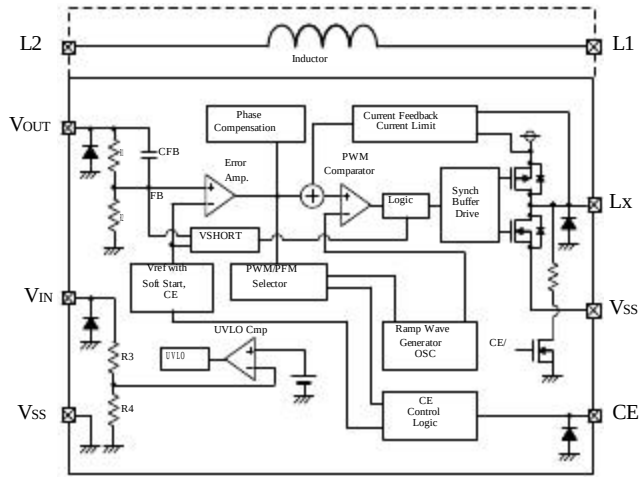
(*1) The "-G" suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

(*2) BR-G is storage temperature range "-40 ℃ ~ + 105 ℃".

(*3) ER-G is storage temperature range "-40 ℃ ~ + 125 ℃".

■BLOCK DIAGRAM

●JTMT201XCLB / JTMT202XCLB Series



NOTE: The JTMT201XCL offers a fixed PWM control, a signal from CE Control Logic to PWM/PFM Selector is fixed to "L" level inside. The JTMT202XCL control scheme is PWM/PFM automatic switching, a signal from CE Control Logic to PWM/PFM Selector is fixed to "H" level inside. The diodes placed inside are ESD protection diodes and parasitic diodes.

■ABSOLUTE MAXIMUM RATINGS

Ta = 25℃

PARAMETER		SYMBOL	RATINGS	UNITS
V_{IN} Pin Voltage		V_{IN}	- 0.3 ~ +6.5	V
Lx Pin Voltage		V_{LX}	- 0.3 ~ V_{IN} + 0.3 ≦ +6.5	V
V_{OUT} Pin Voltage		V_{OUT}	- 0.3 ~ +6.5	V
CE Pin Voltage		V_{CE}	- 0.3 ~ +6.5	V
Lx Pin Current		I_{LX}	±1500	mA
Power Dissipation		Pd	1000(*1)	mW
Operating Ambient Temperature		Topr	- 40~ +85	℃
Storage Temperature(*2)	CL-2025	Tstg	- 40 ~ +105	℃
	CL-2025-02		- 40 ~ +125	

(*1) The power dissipation figure shown is PCB mounted (40mm×40mm, t=1.6mm, Glass Epoxy FR-4).
Please refer to page 12 for details.

(*2) Storage temperature, are divided by the product specification of the package.

■ELECTRICAL CHARACTERISTICS

JTMT201XCLB121BR/JTMT202XCLB121BR/JTMT201XCLB121ER/JTMT202XCLB121ER, V_{OUT}=1.2V, f_{OSC}=1.2MHz, Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Output Voltage	V_{OUT}	When connected to external components, V_{IN}=V_{CE}=5.0V, I_{OUT}=30mA	1.176	1.200	1.224	V	①
Operating Voltage Range	V_{IN}		2.0	-	6.0	V	①
Maximum Output Current	I_{OUTMAX}	V_{IN}=$V_{OUT(T)}$+2.0V, V_{CE}=1.0V When connected to external components (*8)	400	-	-	mA	①
UVLO Voltage	V_{UVLO}	V_{CE}=V_{IN}, V_{OUT}=0V Voltage which Lx pin holding "L" level (*1, *10)	1.00	1.40	1.78	V	②
Supply Current (JTMT201)	I_{DD}	V_{IN}=V_{CE}=5.0V, V_{OUT}=$V_{OUT(T)}$×1.1V	-	22	50	μA	②
Supply Current (JTMT202)			-	15	33		
Stand-by Current	I_{STB}	V_{IN}=5.0V, V_{CE}=0V, V_{OUT}= $V_{OUT(T)}$×1.1V	-	0	1.0	μA	③
Oscillation Frequency	f_{OSC}	When connected to external components, V_{IN}=$V_{OUT(T)}$+2.0V, V_{CE}=1.0V , I_{OUT}=100mA	1020	1200	1380	kHz	①
PFM Switching Current (*11)	I_{PFM}	When connected to external components, V_{IN}=$V_{OUT(T)}$+2.0V, V_{CE}=V_{IN} , I_{OUT}=1mA	140	180	240	mA	⑩
PFM Duty Limit (*11)	DTY_{LIMIT_PFM}	V_{CE}=V_{IN} = 2.0V, I_{OUT}=1mA	-	200	300	%	①
Maximum Duty Cycle	MAXDTY	V_{IN}=V_{CE}=5.0V, V_{OUT}=$V_{OUT(T)}$×0.9V	100	-	-	%	③
Minimum Duty Cycle	MINDTY	V_{IN}=V_{CE}=5.0V, V_{OUT}=$V_{OUT(T)}$×1.1V	-	-	0	%	③
Efficiency (*2)	EFFI	When connected to external components, V_{CE}=V_{IN}=$V_{OUT(T)}$+1.2V, I_{OUT}=100mA	-	86	-	%	①
Lx SW "H" ON Resistance 1	R_{LxH1}	V_{IN}=V_{CE}=5.0V, V_{OUT}=0V, I_{LX}=100mA (*3)	-	0.35	0.55	Ω	④
Lx SW "H" ON Resistance 2	R_{LxH2}	V_{IN}=V_{CE}=3.6V, V_{OUT}=0V, I_{LX}=100mA (*3)	-	0.42	0.67	Ω	④
Lx SW "L" ON Resistance 1	R_{LxL1}	V_{IN}=V_{CE}=5.0V (*4)	-	0.45	0.65	Ω	-
Lx SW "L" ON Resistance 2	R_{LxL2}	V_{IN}=V_{CE}=3.6V (*4)	-	0.52	0.77	Ω	-
Lx SW "H" Leakage Current (*5)	I_{LeakH}	V_{IN}=V_{OUT}=5.0V, V_{CE}=0V, L_X=0V	-	0.01	1.0	μA	⑨
Current Limit (*9)	I_{LIM}	V_{IN}=V_{CE}=5.0V, V_{OUT}=$V_{OUT(T)}$×0.9V (*7)	700	800	1000	mA	⑥
Output Voltage Temperature Characteristics	ΔV_{OUT}/ (V_{OUT}・ΔTopr)	I_{OUT}=30mA -40℃≦Topr≦85℃	-	±100	-	ppm/ ℃	①
CE "H" Voltage	V_{CEH}	V_{OUT}=0V, Applied voltage to V_{CE}, Voltage changes Lx to "H" level (*10)	0.65	-	6.0	V	③
CE "L" Voltage	V_{CEL}	V_{OUT}=0V, Applied voltage to V_{CE}, Voltage changes Lx to "L" level (*10)	V_{SS}	-	0.25	V	③
CE "H" Current	I_{CEH}	V_{IN}=V_{CE}=5.0V, V_{OUT}=0V	- 0.1	-	0.1	μA	⑤
CE "L" Current	I_{CEL}	V_{IN}=5.0V, V_{CE}=0V, V_{OUT}=0V	- 0.1	-	0.1	μA	⑤
Soft Start Time	t_{SS}	When connected to external components, V_{CE}=0V→V_{IN} , I_{OUT}=1mA	-	0.25	0.40	ms	①
Latch Time	t_{LAT}	V_{IN}=V_{CE}=5.0V, V_{OUT}=0.8×$V_{OUT(T)}$ Short Lx at 1Ω resistance (*6)	1.0	-	20	ms	⑦
Short Protection Threshold Voltage	V_{SHORT}	Sweeping V_{OUT}, V_{IN}=V_{CE}=5.0V, Short Lx at 1Ω resistance, V_{OUT} voltage which Lx becomes "L" level within 1ms	0.450	0.600	0.750	V	⑦
C_L Discharge	R_{DCHG}	V_{IN}=5.0V, L_X=5.0V, V_{CE}=0V, V_{OUT}=open	200	300	450	Ω	⑧
Inductance Value	L	Test frequency=1MHz	-	4.7	-	μH	-
Allowed Inductor Current	I_{DC}	ΔT=40℃	-	600	-	mA	-

Test conditions: Unless otherwise stated, V_{IN}=5.0V, $V_{OUT(T)}$=Nominal Voltage

NOTE:

(*1) Including hysteresis operating voltage range.

(*2) EFFI= { (output voltage×output current) / (input voltage×input current) }×100

(*3) ON resistance (Ω)=(V_{IN} - Lx pin measurement voltage) / 100mA

(*4) Design value

(*5) When temperature is high, a current of approximately 10μA (maximum) may leak.

(*6) Time until it short-circuits V_{OUT} with GND via 1Ω of resistor from an operational state and is set to Lx=0V from current limit pulse generating.

(*7) When V_{IN} is less than 2.4V, limit current may not be reached because voltage falls caused by ON resistance.

(*8) When the difference between the input and the output is small, some cycles may be skipped completely before current maximizes. If current is further pulled from this state, output voltage will decrease because of P-ch driver ON resistance.

(*9) Current limit denotes the level of detection at peak of coil current.

(*10) "H"=V_{IN}~V_{IN}-1.2V, "L"=+0.1V~-0.1V

(*11) I_{PFM} and DTY_{LIMIT_PFM} are defined only for the JTMT202XCL series which have PFM control function. (Not for the JTMT201XCL series)

■ELECTRICAL CHARACTERISTICS (Continued)

JTMT201XCLB181BR/JTMT202XCLB181BR/JTMT201XCLB181ER/JTMT202XCLB181ER ,V_{OUT}=1.8V, f_{OSC}=1.2MHz, Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Output Voltage	V_{OUT}	When connected to external components, V_{IN}=V_{CE}=5.0V, I_{OUT}=30mA	1.764	1.800	1.836	V	①
Operating Voltage Range	V_{IN}		2.0	-	6.0	V	①
Maximum Output Current	I_{OUTMAX}	V_{IN}=$V_{OUT(E)}$+2.0V, V_{CE}=1.0V When connected to external components (*8)	400	-	-	mA	①
UVLO Voltage	V_{UVLO}	V_{CE}=V_{IN},V_{OUT}=0V Voltage which Lx pin holding "L" level (*1, *10)	1.00	1.40	1.78	V	②
Supply Current (JTMT201)	I_{DD}	V_{IN}=V_{CE}=5.0V, V_{OUT}=$V_{OUT(T)}$×1.1V	-	22	50	μA	②
Supply Current (JTMT202)			-	15	33		
Stand-by Current	I_{STB}	V_{IN}=5.0V, V_{CE}=0V, V_{OUT}=$V_{OUT(T)}$×1.1V	-	0	1.0	μA	③
Oscillation Frequency	f_{OSC}	When connected to external components, V_{IN}=$V_{OUT(T)}$+2.0V, V_{CE}=1.0V , I_{OUT}=100mA	1020	1200	1380	kHz	①
PFM Switching Current (*11)	I_{PFM}	When connected to external components, V_{IN}=$V_{OUT(T)}$+2.0V, V_{CE}=V_{IN} , I_{OUT}=1mA	120	160	200	mA	⑩
PFM Duty Limit (*11)	DTY_{LIMIT_PFM}	V_{CE}=V_{IN}=$V_{OUT(T)}$ +0.5V, I_{OUT}=1mA	-	200	300	%	①
Maximum Duty Cycle	MAXDTY	V_{IN}=V_{CE}=5.0V, V_{OUT}=$V_{OUT(T)}$×0.9V	100	-	-	%	③
Minimum Duty Cycle	MINDTY	V_{IN}=V_{CE}=5.0V, V_{OUT}=$V_{OUT(T)}$×1.1V	-	-	0	%	③
Efficiency (*2)	EFFI	When connected to external components, V_{CE}=V_{IN}=$V_{OUT(T)}$+1.2V, I_{OUT}=100mA	-	89	-	%	①
Lx SW "H" ON Resistance 1	R_{LXH1}	V_{IN}=V_{CE}=5.0V, V_{OUT}=0V, I_{LX}=100mA (*3)	-	0.35	0.55	Ω	④
Lx SW "H" ON Resistance 2	R_{LXH2}	V_{IN}=V_{CE}=3.6V, V_{OUT}=0V, I_{LX}=100mA (*3)	-	0.42	0.67	Ω	④
Lx SW "L" ON Resistance 1	R_{LXL1}	V_{IN}=V_{CE}=5.0V (*4)	-	0.45	0.65	Ω	-
Lx SW "L" ON Resistance 2	R_{LXL2}	V_{IN}=V_{CE}=3.6V (*4)	-	0.52	0.77	Ω	-
Lx SW "H" Leakage Current (*5)	I_{LeakH}	V_{IN}=V_{OUT}=5.0V, V_{CE}=0V, L_X=0V	-	0.01	1.0	μA	⑨
Current Limit (*9)	I_{LIM}	V_{IN}=V_{CE}= 5.0V, V_{OUT}=$V_{OUT(T)}$×0.9V (*7)	700	800	1000	mA	⑥
Output Voltage Temperature Characteristics	ΔV_{OUT}/ (V_{OUT}・ΔTopr)	I_{OUT}=30mA -40℃≦Topr≦85℃	-	±100	-	ppm/ ℃	①
CE "H" Voltage	V_{CEH}	V_{OUT}=0V, Applied voltage to V_{CE}, Voltage changes Lx to "H" level (*10)	0.65	-	6.0	V	③
CE "L" Voltage	V_{CEL}	V_{OUT}=0V, Applied voltage to V_{CE}, Voltage changes Lx to "L" level (*10)	V_{SS}	-	0.25	V	③
CE "H" Current	I_{CEH}	V_{IN}=V_{CE}=5.0V, V_{OUT}=0V	- 0.1	-	0.1	μA	⑤
CE "L" Current	I_{CEL}	V_{IN}=5.0V, V_{CE}=0V, V_{OUT}=0V	- 0.1	-	0.1	μA	⑤
Soft Start Time	t_{SS}	When connected to external components, V_{CE}=0V→V_{IN} , I_{OUT}=1mA	-	0.32	0.50	ms	①
Latch Time	t_{LAT}	V_{IN}=V_{CE}=5.0V, V_{OUT}=0.8×$V_{OUT(T)}$ Short Lx at 1Ω resistance (*6)	1.0	-	20	ms	⑦
Short Protection Threshold Voltage	V_{SHORT}	Sweeping V_{OUT}, V_{IN}=V_{CE}=5.0V, Short Lx at 1Ω resistance, V_{OUT} voltage which Lx becomes "L" level within 1ms	0.675	0.900	1.125	V	⑦
C_L Discharge	R_{DCHG}	V_{IN}=5.0V L_X=5.0V V_{CE}=0V V_{OUT}=open	200	300	450	Ω	⑧
Inductance Value	L	Test frequency=1MHz	-	4.7	-	μH	-
Allowed Inductor Current	I_{DC}	ΔT=40℃	-	600	-	mA	-

Test conditions: Unless otherwise stated, V_{IN}=5.0V, $V_{OUT(T)}$=Nominal Voltage

NOTE:

(*1) Including hysteresis operating voltage range.

(*2) EFFI={ (output voltage×output current) / (input voltage×input current) }×100

(*3) ON resistance (Ω)=(V_{IN} - Lx pin measurement voltage) / 100mA

(*4) Design value

(*5) When temperature is high, a current of approximately 10μA (maximum) may leak.

(*6) Time until it short-circuits V_{OUT} with GND via 1Ω of resistor from an operational state and is set to Lx=0V from current limit pulse generating.

(*7) When V_{IN} is less than 2.4V, limit current may not be reached because voltage falls caused by ON resistance.

(*8) When the difference between the input and the output is small, some cycles may be skipped completely before current maximizes. If current is further pulled from this state, output voltage will decrease because of P-ch driver ON resistance.

(*9) Current limit denotes the level of detection at peak of coil current.

(*10) "H"=V_{IN}~V_{IN}-1.2V, "L"=+0.1V~-0.1V

(*11) I_{PFM} and DTY_{LIMIT_PFM} are defined only for the JTMT202 series which have PFM control function. (Not for the JTMT201 series)

■ELECTRICAL CHARACTERISTICS (Continued)

The value and conditions are depends on setting output voltage.

●PFM Switching Current (I_{PFM}) (JTMT202XCL)

NOMINAL OUTPUT VOLTAGE	MIN.	TYP.	MAX.
0.8V≦$V_{OUT(T)}$ ≦1.2V	140mA	180mA	240mA
1.2V＜$V_{OUT(T)}$＜1.8V	130mA	170mA	220mA
1.8V≦$V_{OUT(T)}$≦4.0V	120mA	160mA	200mA

●PFM Duty Limit DTY_{LIMIT_PFM} (JTMT202XCL)

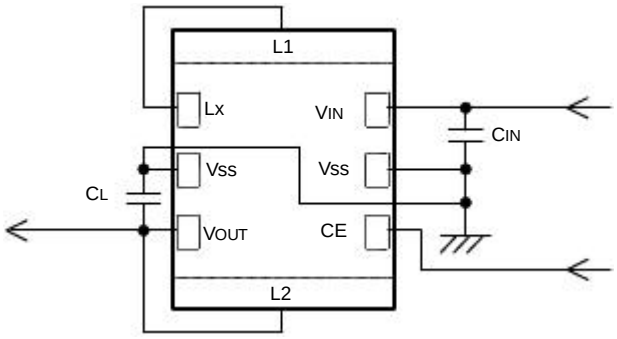
SETTING VOLTAGE	CONDITIONS
0.8V≦$V_{OUT(T)}$＜1.0V	V_{CE}=V_{IN}=2.0V, I_{OUT}=1mA
1.0V≦$V_{OUT(T)}$≦4.0V	V_{CE}=V_{IN}=$V_{OUT(T)}$+0.5V, I_{OUT}=1mA

●Soft-Start Time t_{SS}

SERIES	OUTPUT VOLTAGE	MIN.	TYP.	MAX.
JTMT201B	0.8V≦$V_{OUT(T)}$＜1.5V	-	0.25ms	0.40ms
	1.5V≦$V_{OUT(T)}$＜1.8V	-	0.32ms	0.50ms
	1.8V≦$V_{OUT(T)}$＜2.5V	-	0.28ms	0.40ms
	2.5V≦$V_{OUT(T)}$≦4.0V	-	0.32ms	0.50ms
JTMT202B	0.8V≦$V_{OUT(T)}$＜2.5V	-	0.28ms	0.40ms
	2.5V≦$V_{OUT(T)}$≦4.0V	-	0.32ms	0.50ms

■TYPICAL APPLICATION CIRCUIT

JTMT201XCL/JTMT202XCL Series



●External Components

C_{IN} : 10V/4.7μF(Ceramic)

C_L : 6.3V/10μF(Ceramic)

NOTE:

The Inductor can be used only for this DC/DC converter.

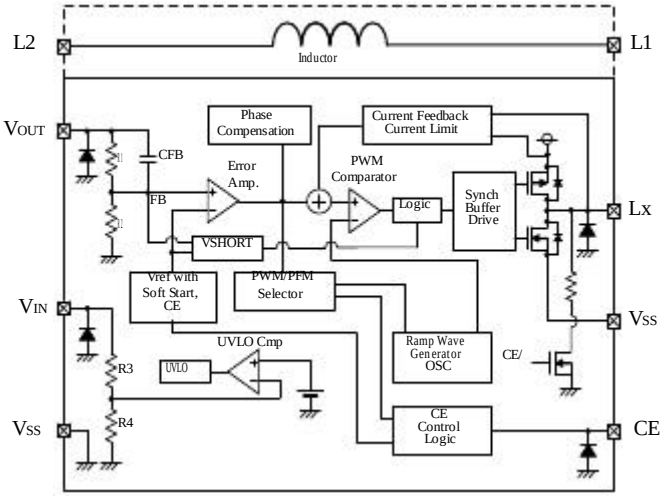
Please do not use this inductor for the other reasons.

Please use B, X5R, and X7R grades in temperature characteristics for C_{IN} and C_L capacitors.

These grade ceramic capacitors minimize capacitance-loss as a function of voltage stress.

■OPERATIONAL DESCRIPTION

The JTMT201XCL/JTMT202XCL series consists of a reference voltage source, ramp wave circuit, error amplifier, PWM comparator, phase compensation circuit, output voltage adjustment resistors, P-channel MOSFET driver transistor, N-channel MOSFET switching transistor for the synchronous switch, current limiter circuit, UVLO circuit with control IC, and an inductor. (See the block diagram below.) Using the error amplifier, the voltage of the internal voltage reference source is compared with the feedback voltage from the V_{OUT} pin through split resistors, R1 and R2. Phase compensation is performed on the resulting error amplifier output, to input a signal to the PWM comparator to determine the turn-on time during PWM operation. The PWM comparator compares, in terms of voltage level, the signal from the error amplifier with the ramp wave from the ramp wave circuit, and delivers the resulting output to the buffer driver circuit to cause the Lx pin to output a switching duty cycle. This process is continuously performed to ensure stable output voltage. The current feedback circuit monitors the P-channel MOS driver transistor current for each switching operation, and modulates the error amplifier output signal to provide multiple feedback signals. This enables a stable feedback loop even when a low ESR capacitor such as a ceramic capacitor is used ensuring stable output voltage.



<Reference Voltage Source>
The reference voltage source provides the reference voltage to ensure stable output voltage of the DC/DC converter.

<Ramp Wave Circuit>
The ramp wave circuit determines switching frequency. The frequency is fixed internally 1.2MHz. Clock pulses generated in this circuit are used to produce ramp waveforms needed for PWM operation, and to synchronize all the internal circuits.

<Error Amplifier>
The error amplifier is designed to monitor output voltage. The amplifier compares the reference voltage with the feedback voltage divided by the internal split resistors, R1 and R2. When a feed back voltage is lower than the reference voltage, the output voltage of the error amplifier is increased. The gain and frequency characteristics of the error amplifier output are fixed internally to deliver an optimized signal to the mixer.

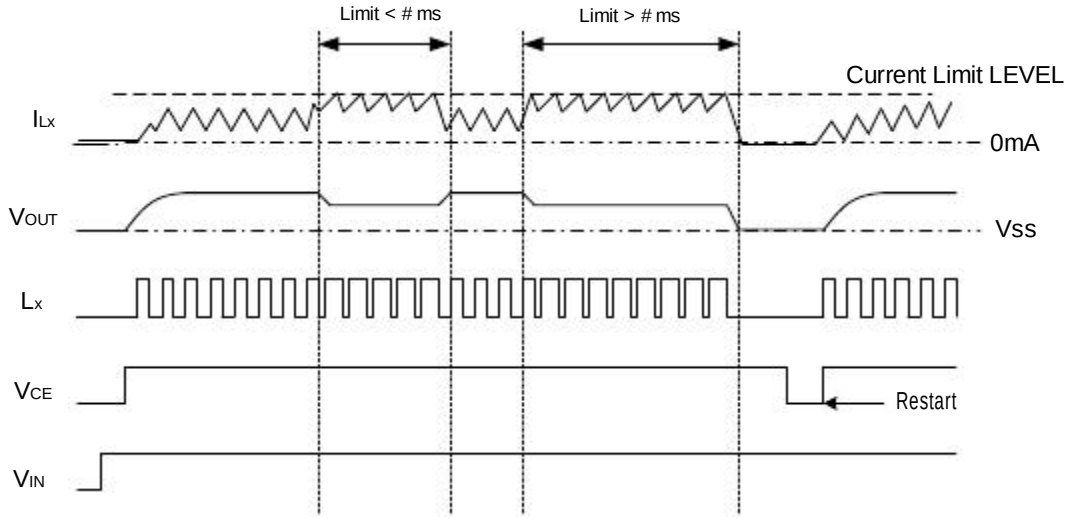
■OPERATIONAL DESCRIPTION (Continued)

<Current Limit>

The current limiter circuit of the JTMT201XCL/JTMT202XCL series monitors the current flowing through the P-channel MOS driver transistor connected to the Lx pin, and features a combination of the current limit mode and the operation suspension mode.

- When the driver current is greater than a specific level, the current limit function operates to turn off the pulses from the Lx pin at any given timing.
- When the driver transistor is turned off, the limiter circuit is then released from the current limit detection state.
- At the next pulse, the driver transistor is turned on. However, the transistor is immediately turned off in the case of an over current state.
- When the over current state is eliminated, the IC resumes its normal operation.

The IC waits for the over current state to end by repeating the steps ① through ③. If an over current state continues for a few milliseconds and the above three steps are repeatedly performed, the IC performs the function of latching the OFF state of the driver transistor, and goes into operation suspension state. Once the IC is in suspension state, operations can be resumed by either turning the IC off via the CE pin, or by restoring power to the V_{IN} pin. The suspension state does not mean a complete shutdown, but a state in which pulse output is suspended; therefore, the internal circuitry remains in operation. The current limit of the JTMT201XCL/JTMT202XCL series can be set at 800mA at typical. Depending on the state of the PC Board, latch time may become longer and latch operation may not work. In order to avoid the effect of noise, an input capacitor is placed as close to the IC as possible.



<Short-Circuit Protection>

The short-circuit protection circuit monitors the internal R1 and R2 divider voltage from the V_{OUT} pin (refer to FB point in the block diagram shown in the previous page). In case where output is accidentally shorted to the Ground and when the FB point voltage decreases less than half of the reference voltage (Vref) and a current more than the I_{LIM} flows to the driver transistor, the short-circuit protection quickly operates to turn off and to latch the driver transistor. In the latch state, the operation can be resumed by either turning the IC off and on via the CE pin, or by restoring power supply to the V_{IN} pin.

When sharp load transient happens, a voltage drop at the V_{OUT} is propagated to the FB point through C_{FB}, as a result, short circuit protection may operate in the voltage higher than 1/2 V_{OUT} voltage.

<UVLO Circuit>

When the V_{IN} pin voltage becomes 1.4V or lower, the P-channel output driver transistor is forced OFF to prevent false pulse output caused by unstable operation of the internal circuitry. When the V_{IN} pin voltage becomes 1.8V or higher, switching operation takes place. By releasing the UVLO function, the IC performs the soft start function to initiate output startup operation. The soft start function operates even when the VIN pin voltage falls momentarily below the UVLO operating voltage. The UVLO circuit does not cause a complete shutdown of the IC, but causes pulse output to be suspended; therefore, the internal circuitry remains in operation.

■OPERATIONAL DESCRIPTION (Continued)

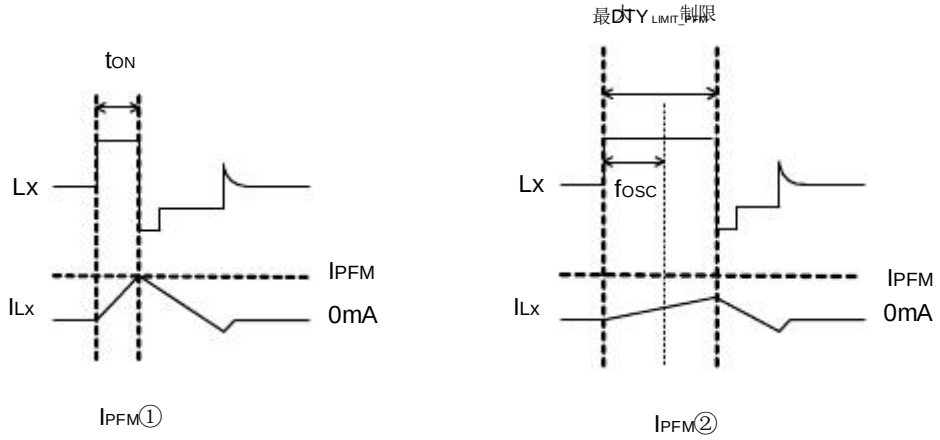
<PFM Switch Current>

In PFM control operation, until coil current reaches to a specified level (I_{PFM}), the IC keeps the P-ch MOSFET on. In this case, on-time (t_{ON}) that the P-ch MOSFET is kept on can be given by the following formula.

$t_{ON} = L \times I_{PFM} / (V_{IN} - V_{OUT})$ →IPFM①

<PFM Duty Limit>

In the PFM control operation, the PFM Duty Limit (DTY_{LIMIT_PFM}) is set to 200% (TYP.). Therefore, under the condition that the duty increases (e.g. the condition that the step-down ratio is small), it's possible for P-ch MOSFET to be turned off even when coil current doesn't reach to IPFM. →IPFM②



I_{PFM}① I_{PFM}②

<C_L High Speed Discharge>

The JTMT201XCL/JTMT202XCL series can quickly discharge the electric charge at the output capacitor (C_L) when a low signal to the CE pin which enables a whole IC circuit put into OFF state, is inputted via the N-channel transistor located between the L_X pin and the V_{SS} pin. When the IC is disabled, electric charge at the output capacitor (C_L) is quickly discharged so that it may avoid application malfunction. Discharge time of the output capacitor (C_L) is set by the C_L auto-discharge resistance (R) and the output capacitor (C_L). By setting time constant of a C_L auto-discharge resistance value [R] and an output capacitor value (C_L) as τ(τ=C x R), discharge time of the output voltage after discharge via the N channel transistor is calculated by the following formula.

$V = V_{OUT(T)} \times e^{-t/\tau}$ or $t = \tau \ln (V_{OUT(T)} / V)$

V : Output voltage after discharge

$V_{OUT(T)}$: Output voltage

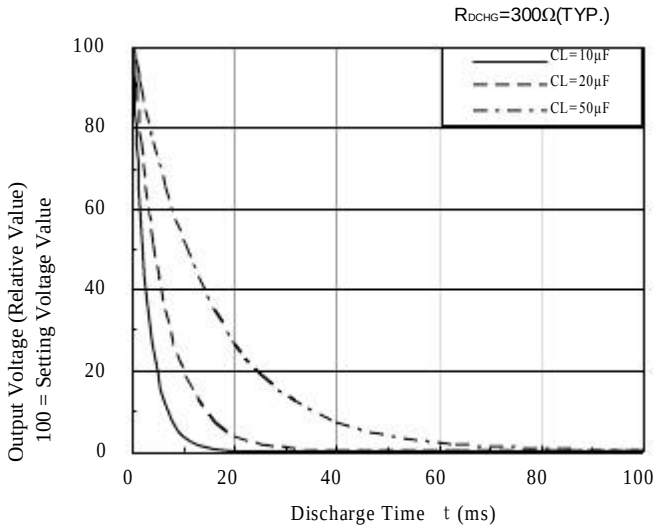
t: Discharge time,

τ: C x R

C=Capacitance of output capacitor (C_L)

R=C_L auto-discharge resistance

Output Voltage Discharge Characteristics

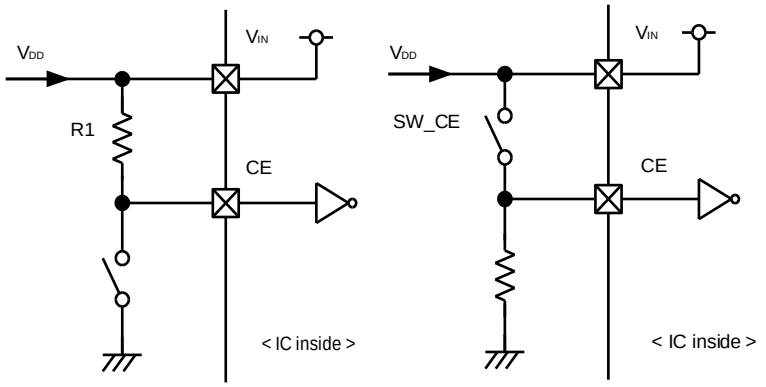


■OPERATIONAL DESCRIPTION (Continued)

<CE Pin Function>

The operation of the JTMT201XCL/JTMT202XCL series will enter into the shut down mode when a low level signal is input to the CE pin. During the shutdown mode, the current consumption of the IC becomes 0μA (TYP.), with a state of high impedance at the Lx pin and V_{OUT} pin. The IC starts its operation by inputting a high level signal to the CE pin. The input to the CE pin is a CMOS input and the sink current is 0μA (TYP.).

●JTMT20/JTMT202XCL series - Examples of how to use CE pin



(A)

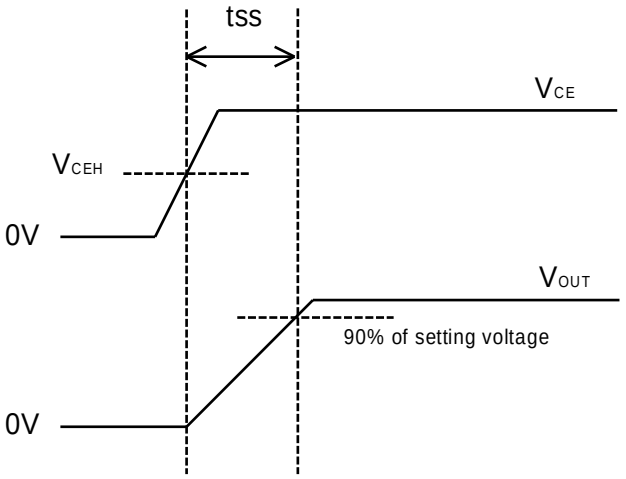
SW_CE	SELECTED STATUS
ON	Stand-by
OFF	Operation

(B)

SW_CE	SELECTED STATUS
ON	Operation
OFF	Stand-by

<Soft Start>

Soft start time is internally set 0.25ms to 0.32ms (TYP). Soft start time is defined as the time to reach 90% of the output nominal voltage when the CE pin is turned on.



■FUNCTION CHART

CE VOLTAGE LEVEL	OPERATIONAL STATES	
	JTMT201	JTMT202
H Level (*1)	Synchronous PWM Fixed Control	Synchronous PWM/PFM Automatic Switching
L Level (*2)	Stand-by	Stand-by

* CE pin voltage level range

- H level: 0.65V<V_{CE}<6V
- L level: 0V<V_{CE}<0.25V
- CE pin should not be left open to avoid unstable operation.

■NOTE ON USE

1. The JTMT201XCL/JTMT202XCL series is designed for use with ceramic output capacitors. If, however, the potential difference is too large between the input voltage and the output voltage, a ceramic capacitor may fail to absorb the resulting high switching energy and oscillation could occur on the output. If the input-output potential difference is large, connect an electrolytic capacitor in parallel to compensate for insufficient capacitance.

2. Spike noise and ripple voltage arise in a switching regulator as with a DC/DC converter. These are greatly influenced by external component selection, such as the coil inductance, capacitance values, and board layout of external components. Once the design has been completed, verification with actual components should be done.

3. Depending on the input-output voltage differential, or load current, some pulses may be skipped, and the ripple voltage may increase.

4. When the difference between input and output is large in PWM control, very narrow pulses will be outputted, and there is the possibility that some cycles may be skipped completely.

5. When the difference between input and output is small, and the load current is heavy, very wide pulses will be outputted and there is the possibility that some cycles may be skipped completely.

6. With the IC, the peak current of the coil is controlled by the current limit circuit. Since the peak current increases when dropout voltage or load current is high, current limit starts operation, and this can lead to instability. When peak current becomes high, please adjust the coil inductance value and fully check the circuit operation. In addition, please calculate the peak current according to the following formula:
   $Ipk = (V_{IN} - V_{OUT}) \times OnDuty / (2 \times L \times f_{OSC}) + I_{OUT}$
   L: Coil Inductance Value
   f_{OSC}: Oscillation Frequency

7. When the peak current which exceeds limit current flows within the specified time, the built-in P-ch driver transistor turns off. During the time until it detects limit current and before the built-in transistor can be turned off, the current for limit current flows; therefore, care must be taken when selecting the rating for the external components such as a coil.

8. When V_{IN} is less than 2.4V, limit current may not be reached because voltage falls caused by ON resistance.

9. Depending on the state of the PC Board, latch time may become longer and latch operation may not work. In order to avoid the effect of noise, the board should be laid out so that input capacitors are placed as close to the IC as possible.

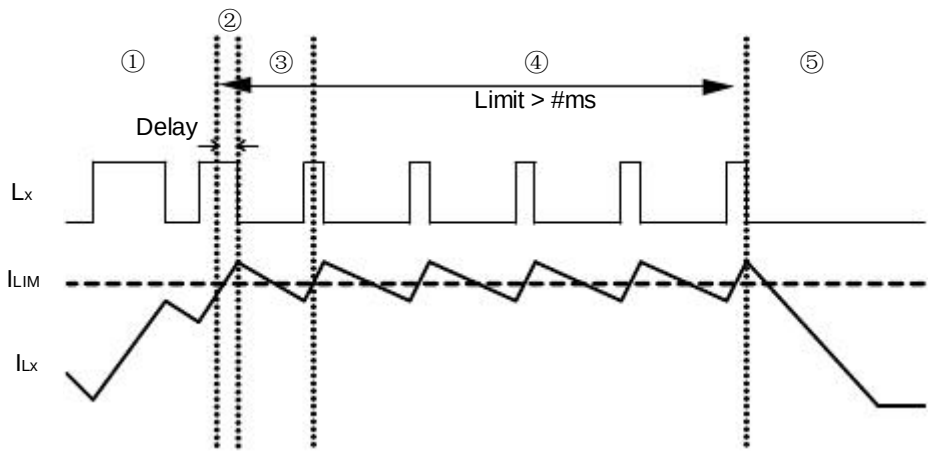
10. Use of the IC at voltages below the recommended voltage range may lead to instability.

11. This IC should be used within the stated absolute maximum ratings in order to prevent damage to the device.

12. When the IC is used in high temperature, output voltage may increase up to input voltage level at no load because of the leak current of the driver transistor.

13. The current limit is set to 1000mA (MAX.) at typical. However, the current of 1000mA or more may flow.
    In case that the current limit functions while the V_{OUT} pin is shorted to the GND pin, when P-ch MOSFET is ON, the potential difference for input voltage will occur at both ends of a coil. For this, the time rate of coil current becomes large. By contrast, when N-ch MOSFET is ON, there is almost no potential difference at both ends of the coil since the V_{OUT} pin is shorted to the GND pin. Consequently, the time rate of coil current becomes quite small. According to the repetition of this operation, and the delay time of the circuit, coil current will be converged on a certain current value, exceeding the amount of current, which is supposed to be limited originally. Even in this case, however, after the over current state continues for several ms, the circuit will be latched. A coil should be used within the stated absolute maximum rating in order to prevent damage to the device.

①Current flows into P-ch MOSFET to reach the current limit (I_{LIM}).
②The current of I_{LIM} or more flows since the delay time of the circuit occurs during from the detection of the current limit to OFF of P-ch MOSFET.
③Because of no potential difference at both ends of the coil, the time rate of coil current becomes quite small.
④Lx oscillates very narrow pulses by the current limit for several ms.
⑤The circuit is latched, stopping its operation.



■NOTE ON USE (Continued)

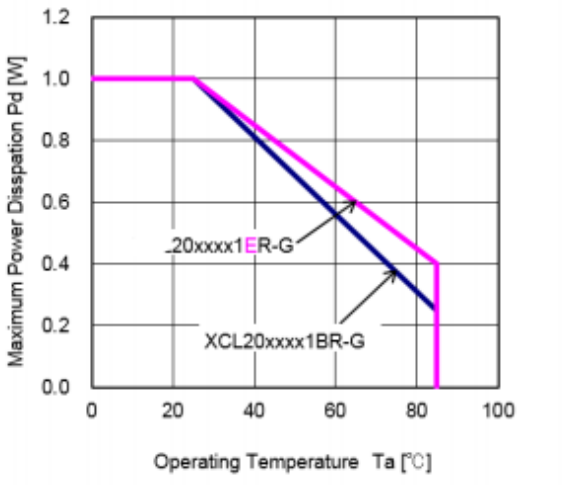
14. In order to stabilize V_{IN} voltage level and oscillation frequency, we recommend that a by-pass capacitor (C_{IN}) be connected as close as possible to the V_{IN} & V_{SS} pins.

15. High step-down ratio and very light load may lead an intermittent oscillation when PWM mode.

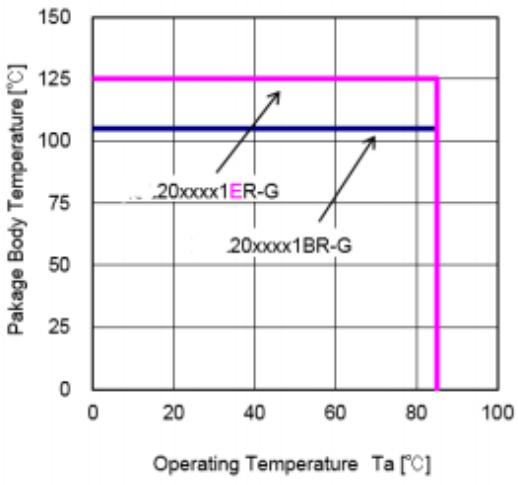
16. When PWM/PFM automatic switching goes into continuous mode, the IC may be in unstable operation for the range of MAXDUTY area with small input/output differential.

17. Please use within the power dissipation range below. Please also note that the power dissipation may changed by test conditions, the power dissipation figure shown is PCB mounted.

Pd vs Operating Temperature



Pakage Body Temperature vs Operating Temperature



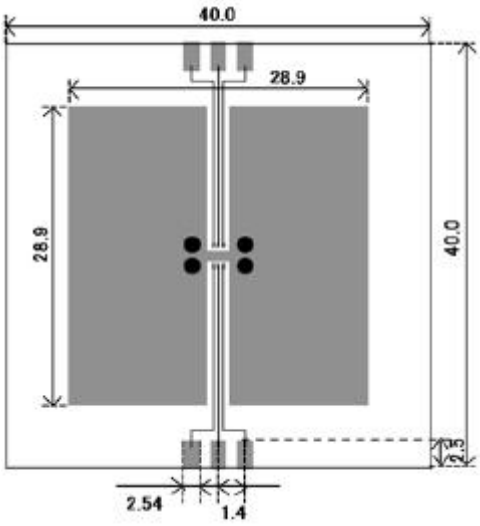
the power loss of micro DC/DC according to the following formula:

power loss = $V_{OUT} \times I_{OUT} \times ((100/EFFI) - 1)$ *(W)*

V_{OUT} : Output Voltage (V)
I_{OUT} : Output Current (A)
EFFI: Conversion Efficiency (%)

Measurement Condition (Reference data)

Condition:	Mount on a board
Ambient:	Natural convection
Soldering:	Lead (Pb) free
Board:	Dimensions 40 x 40 mm (1600 mm_2 in one side)
	Copper (Cu) traces occupy 50% of the board area
	In top and back faces
	Package heat-sink is tied to the copper traces
Material:	Glass Epoxy (FR-4)
Thickness:	1.6mm
Through-hole:	4 x 0.8 Diameter

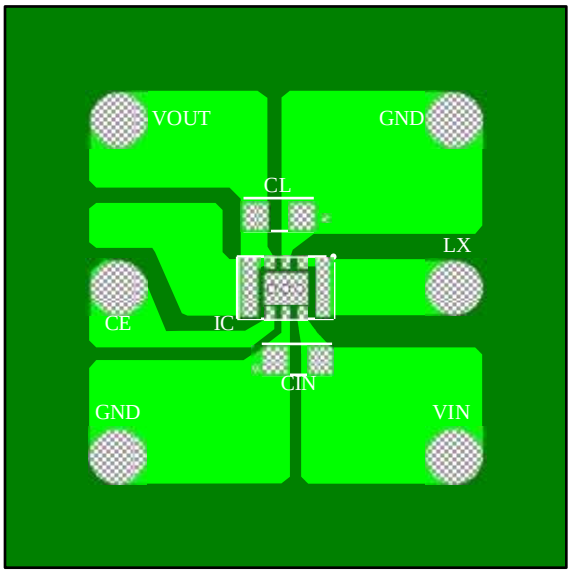


Evaluation Board (unit: mm)

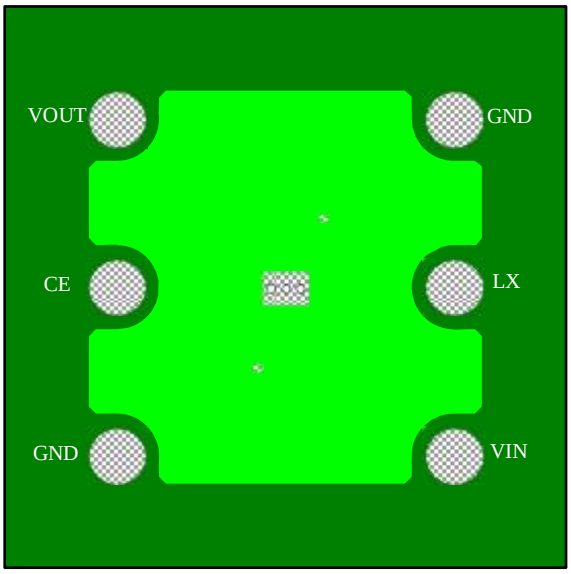
■NOTE ON USE (Continued)

●Instructions of pattern layouts

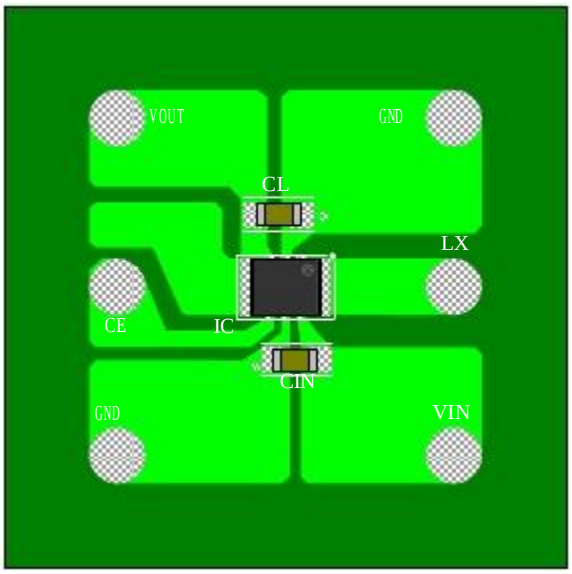
1. In order to stabilize V_{IN} voltage level, we recommend that a by-pass capacitor (C_{IN}) be connected as close as possible to the V_{IN} (No.6) & V_{SS} (No.5) pins.
2. Please mount each external component as close to the IC as possible.
3. Wire external components as close to the IC as possible and use thick, short connecting traces to reduce the circuit impedance.
4. Make sure that the PCB GND traces are as thick as possible, as variations in ground potential caused by high ground currents at the time of switching may result in instability of the IC.
5. This series' internal driver transistors bring on heat because of the output current and ON resistance of driver transistors.
6. Please connect Lx (No.1) pin and L1 (No.7) pin by wiring on the PCB.
7. Please connect V_{OUT} (No.3) pin and L2 (No.8) pin by wiring on the PCB.



FRONT



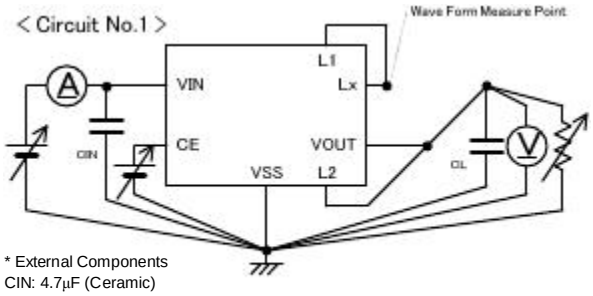
BACK (Flip Horizontal)



FRONT (PCB mounted)

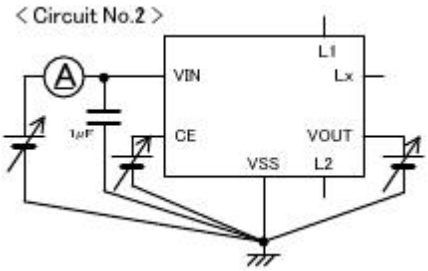
■TEST CIRCUITS

< Circuit No.1 >

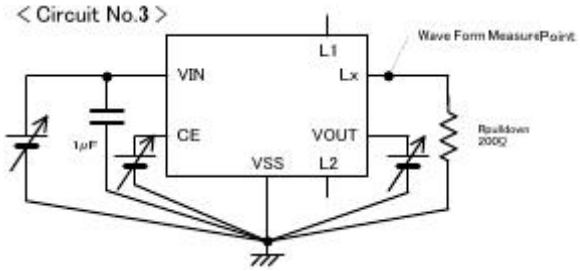


* External Components
CIN: 4.7μF (Ceramic)
CL: 10μF (Ceramic)

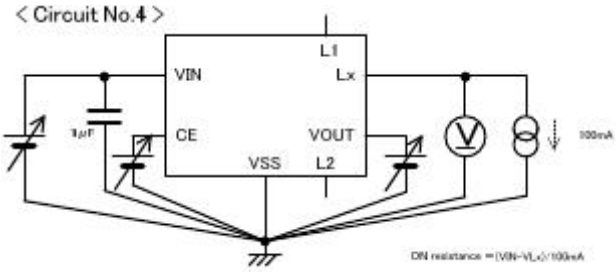
< Circuit No.2 >



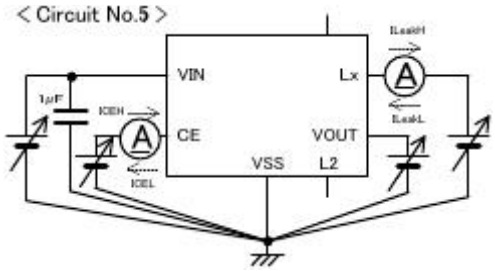
< Circuit No.3 >



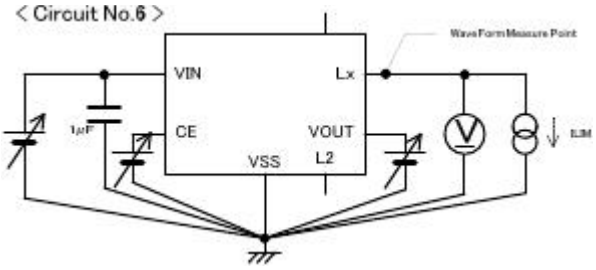
< Circuit No.4 >



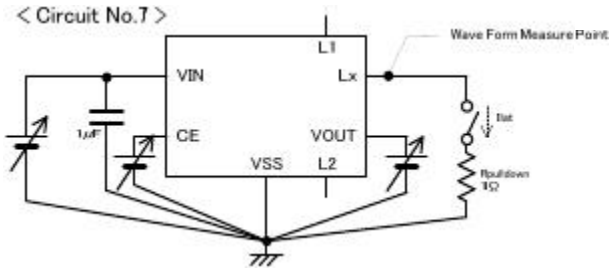
< Circuit No.5 >



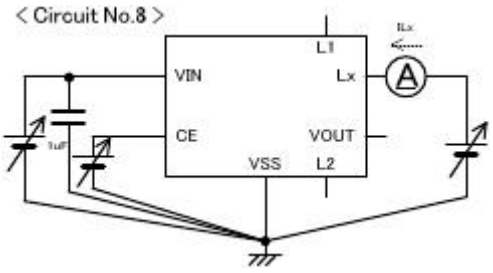
< Circuit No.6 >



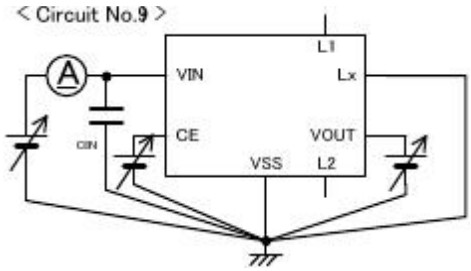
< Circuit No.7 >



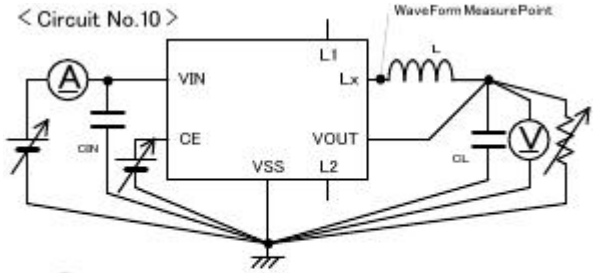
< Circuit No.8 >



< Circuit No.9 >



< Circuit No.10 >

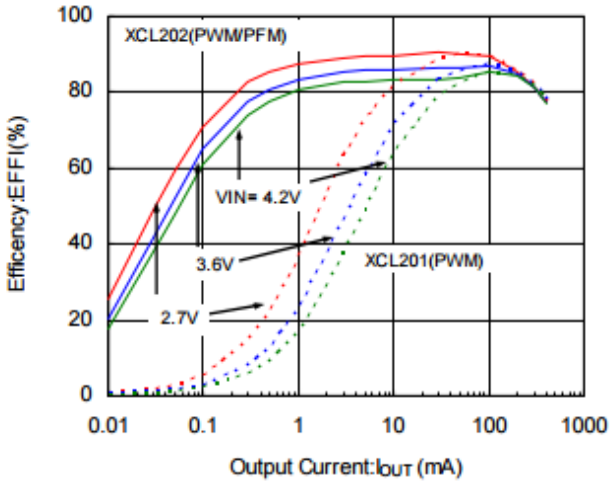


* External Components
L: 4.7μH (Screening Parts)
CIN: 4.7μF (Ceramic)
CL: 10μF (Ceramic)

■TYPICAL PERFORMANCE CHARACTERISTICS

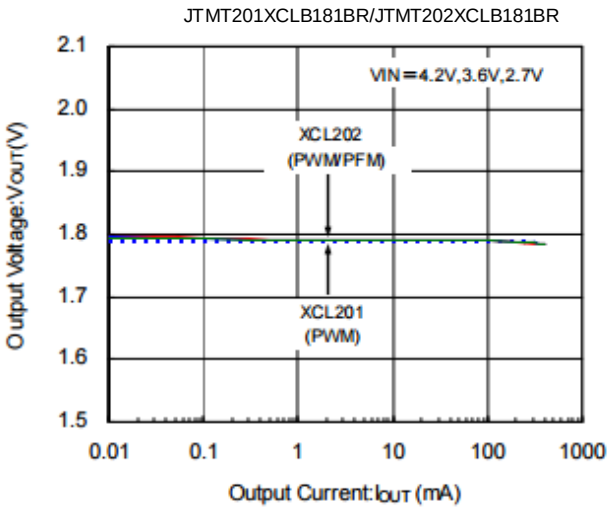
(1) Efficiency vs. Output Current

JTMT201XCLB181BR/JTMT202XCLB181BR



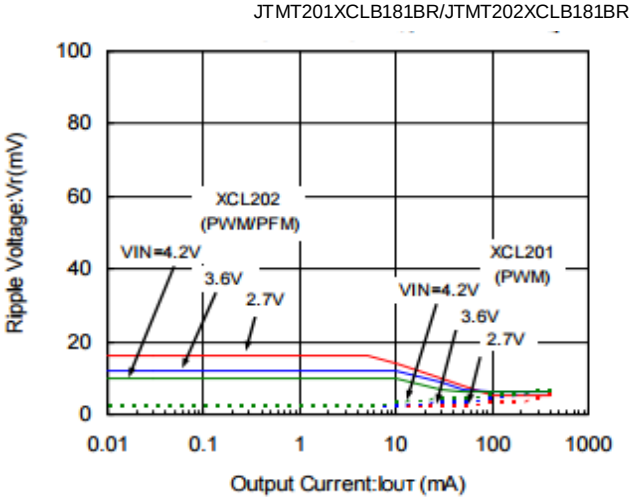
(2) Output Voltage vs. Output Current

JTMT201XCLB181BR/JTMT202XCLB181BR



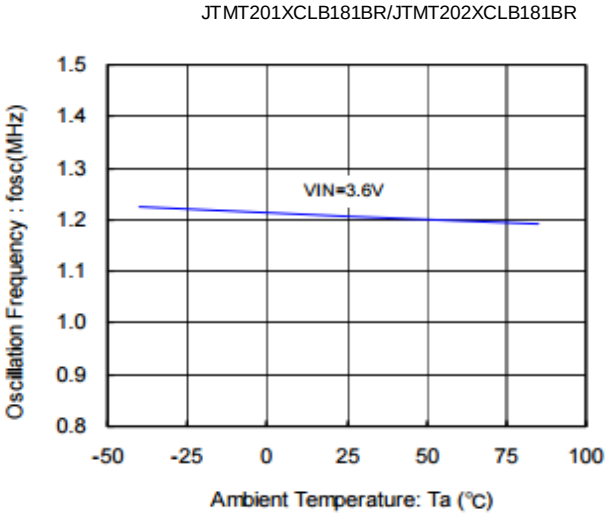
(3) Ripple Voltage vs. Output Current

JTMT201XCLB181BR/JTMT202XCLB181BR



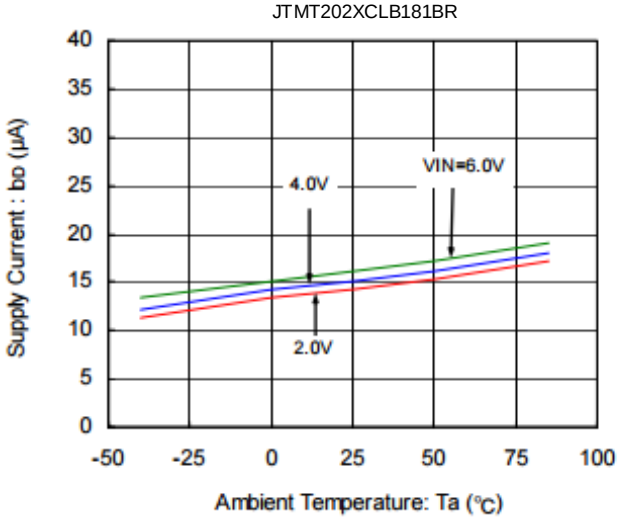
(4) Oscillation Frequency vs. Ambient Temperature

JTMT201XCLB181BR/JTMT202XCLB181BR



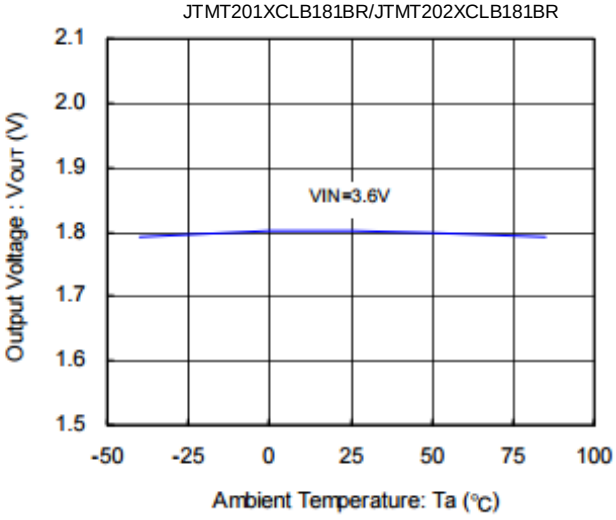
(5) Supply Current vs. Ambient Temperature

JTMT202XCLB181BR



(6) Output Voltage vs. Ambient Temperature

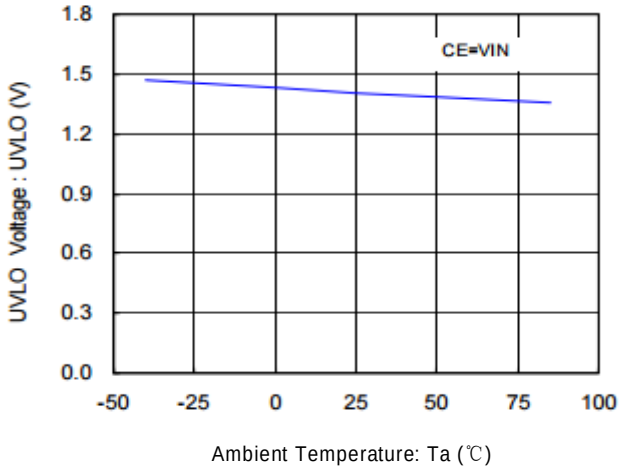
JTMT201XCLB181BR/JTMT202XCLB181BR



■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

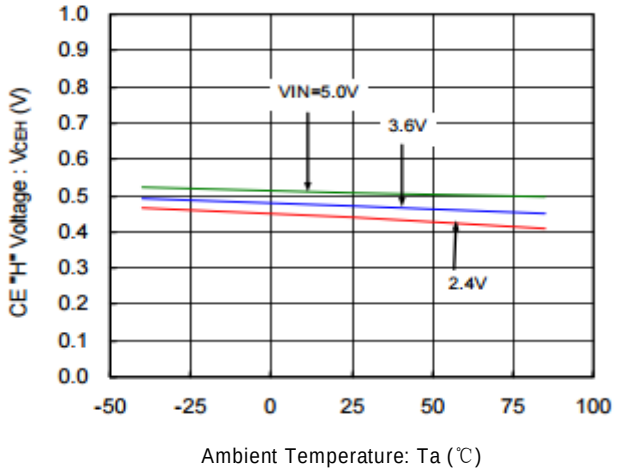
(7) UVLO Voltage vs. Ambient Temperature

JTMT201XCLB181BR/JTMT202XCLB181BR



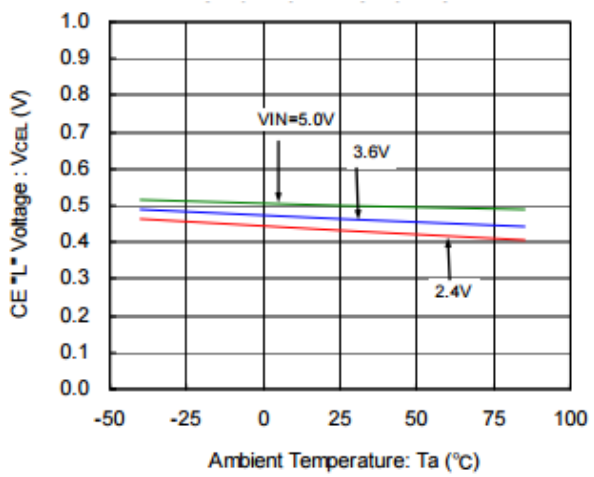
(8) CE "H" Voltage vs. Ambient Temperature

JTMT201XCLB181BR/JTMT202XCLB181BR



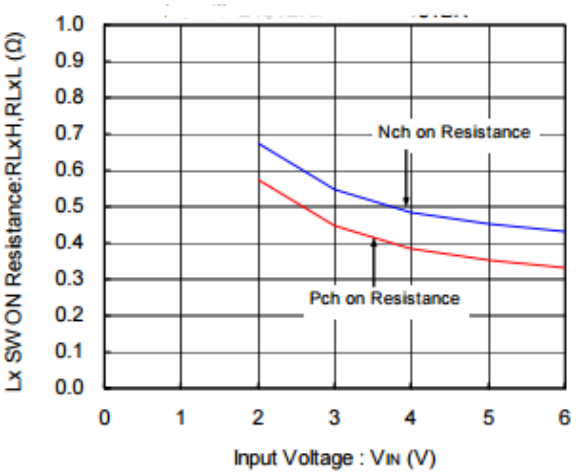
(9) CE "L" Voltage vs. Ambient Temperature

JTMT201XCLB181BR/JTMT202XCLB181BR



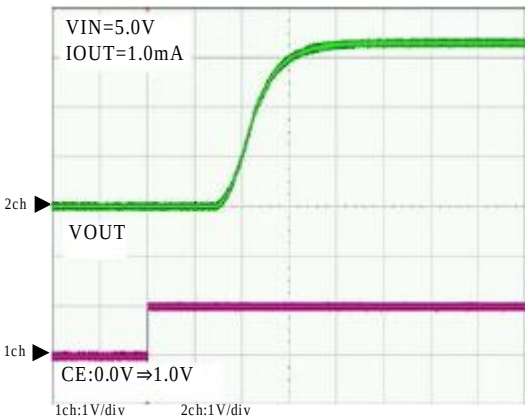
(10) "Pch / Nch" Driver on Resistance vs. Input Voltage

JTMT201XCLB181BR/JTMT202XCLB181BR



(11) Rise Wave Form

JTMT201XCLB331BR/JTMT202XCLB331BR

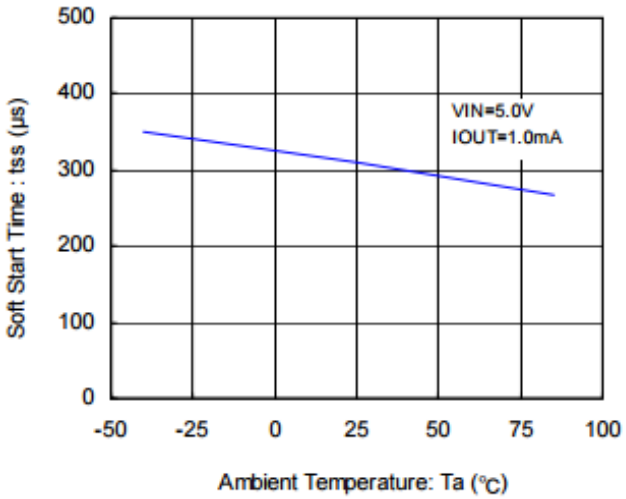


Time:100μs/div

■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

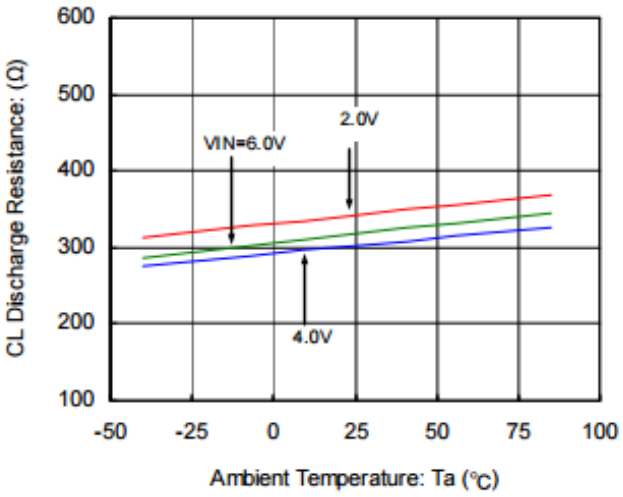
(12) Soft-Start Time vs. Ambient Temperature

JTMT201XCLB121BR/JTMT202XCLB121BR



(13) CL Discharge Resistance vs. Ambient Temperature

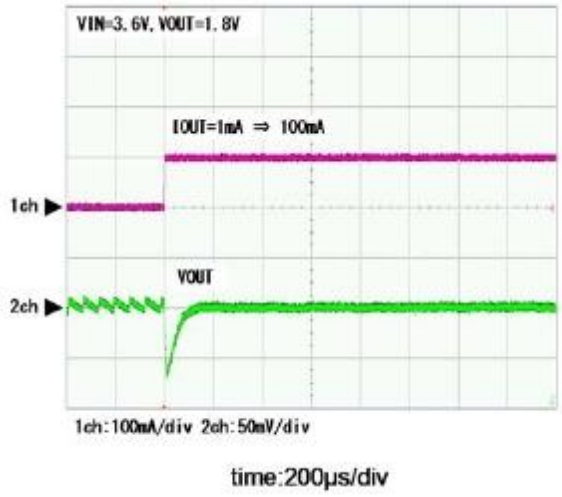
JTMT201XCLB331BR/JTMT202XCLB331BR



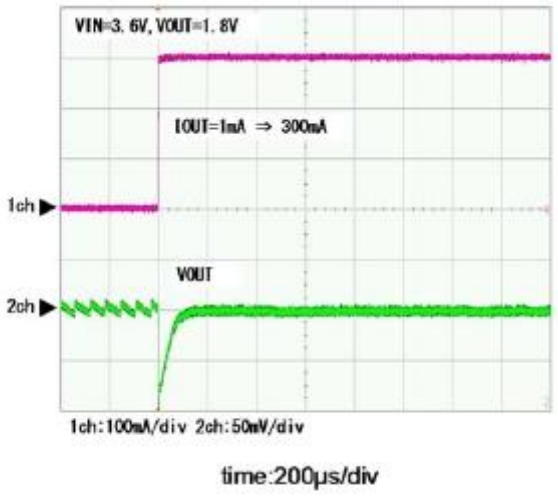
(14) Load Transient Response

MODE：PWM/PFM Automatic Switching Control

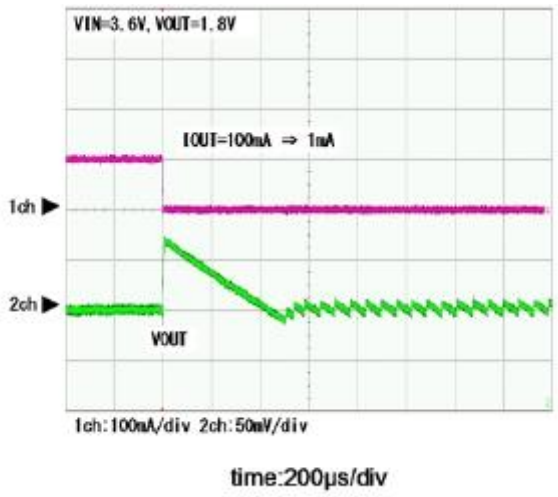
JTMT202XCLB181BR



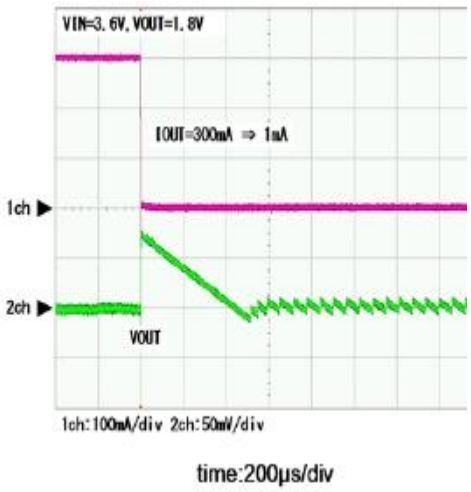
JTMT202XCLB181BR



JTMT202XCLB181BR



JTMT202XCLB181BR

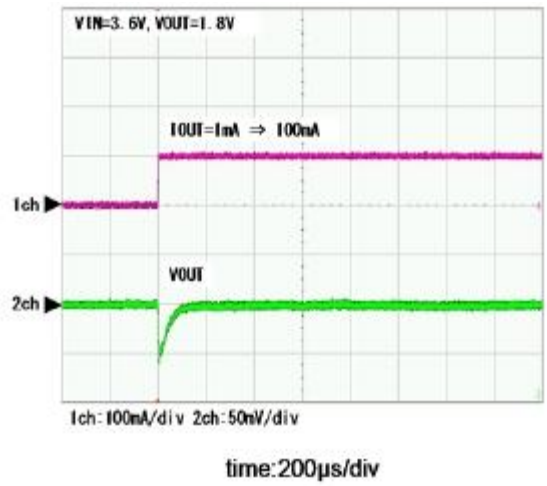


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

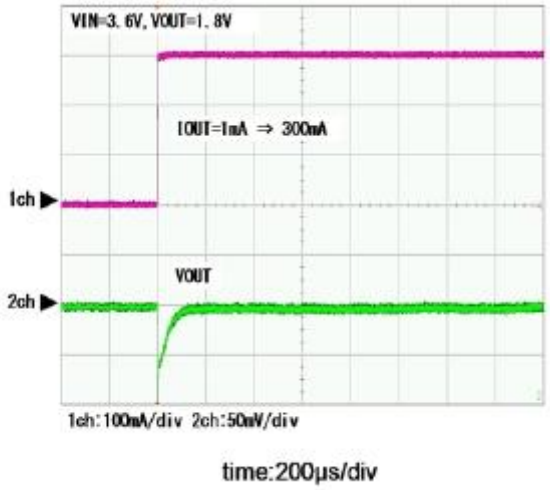
(14) Load Transient Response (Continued)

MODE：PWM Control

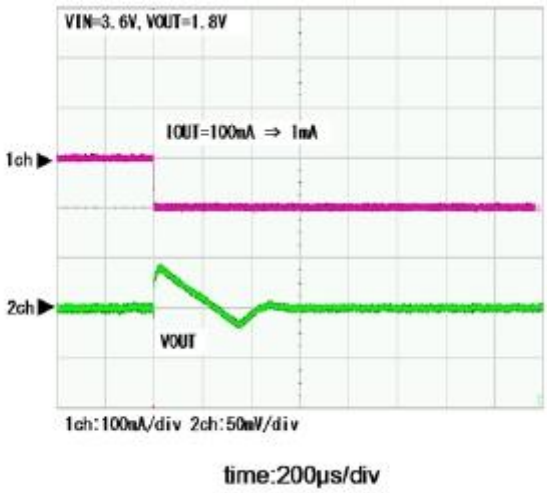
JTMT201XCLB181BR



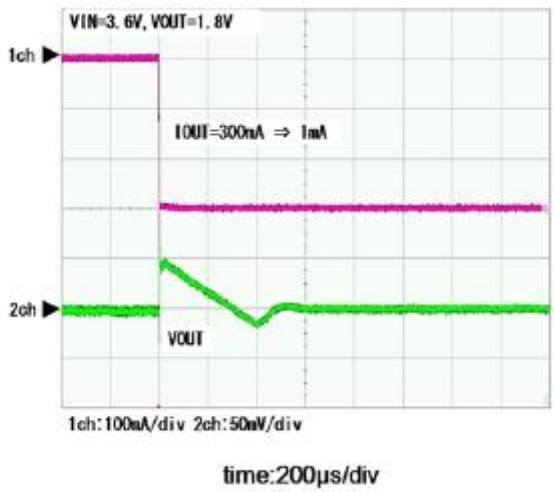
JTMT201XCLB181BR



JTMT201XCLB181BR

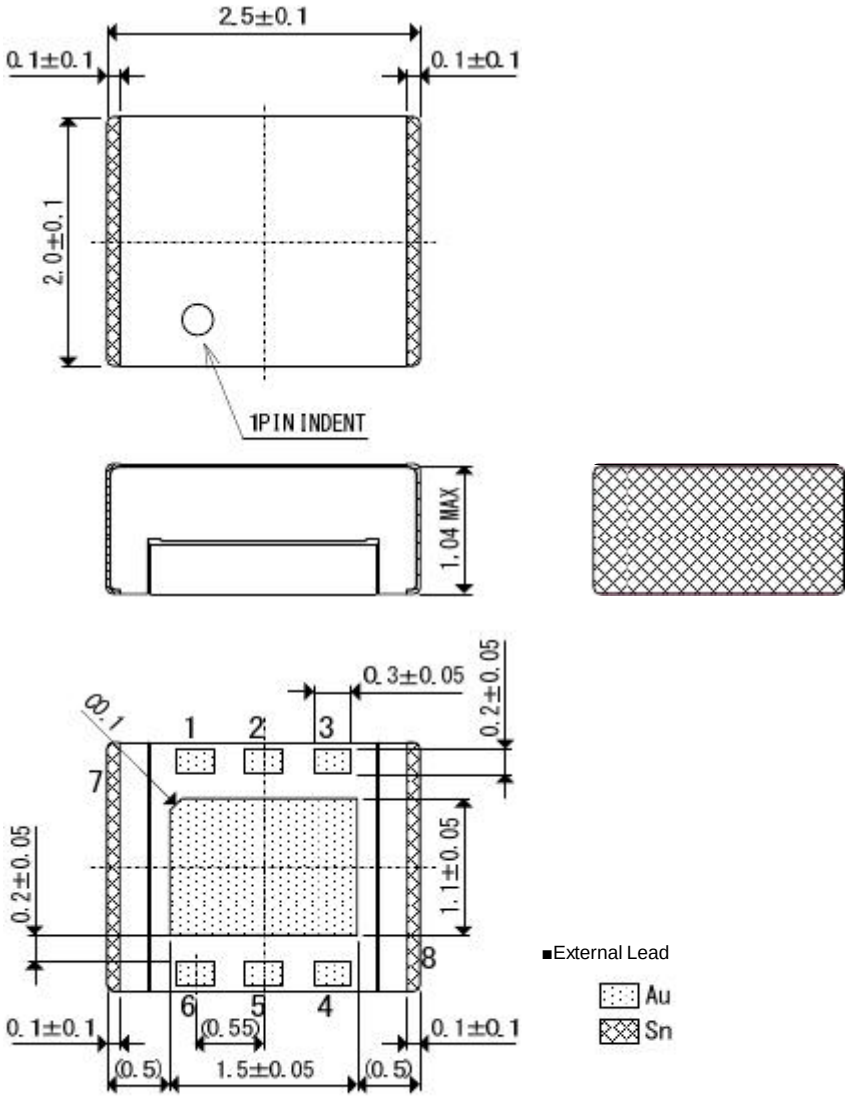


JTMT201XCLB181BR

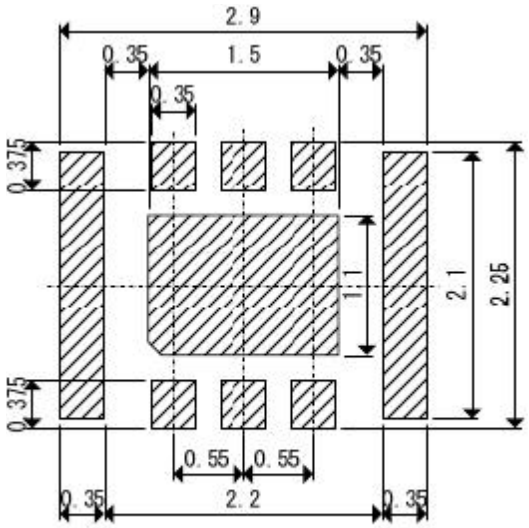


■PACKAGING INFORMATION

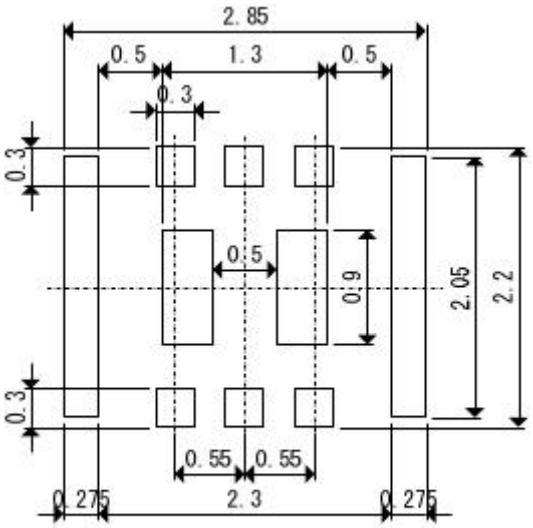
●CL-2025 (unit:mm)



●Reference Pattern Layout (unit:mm)

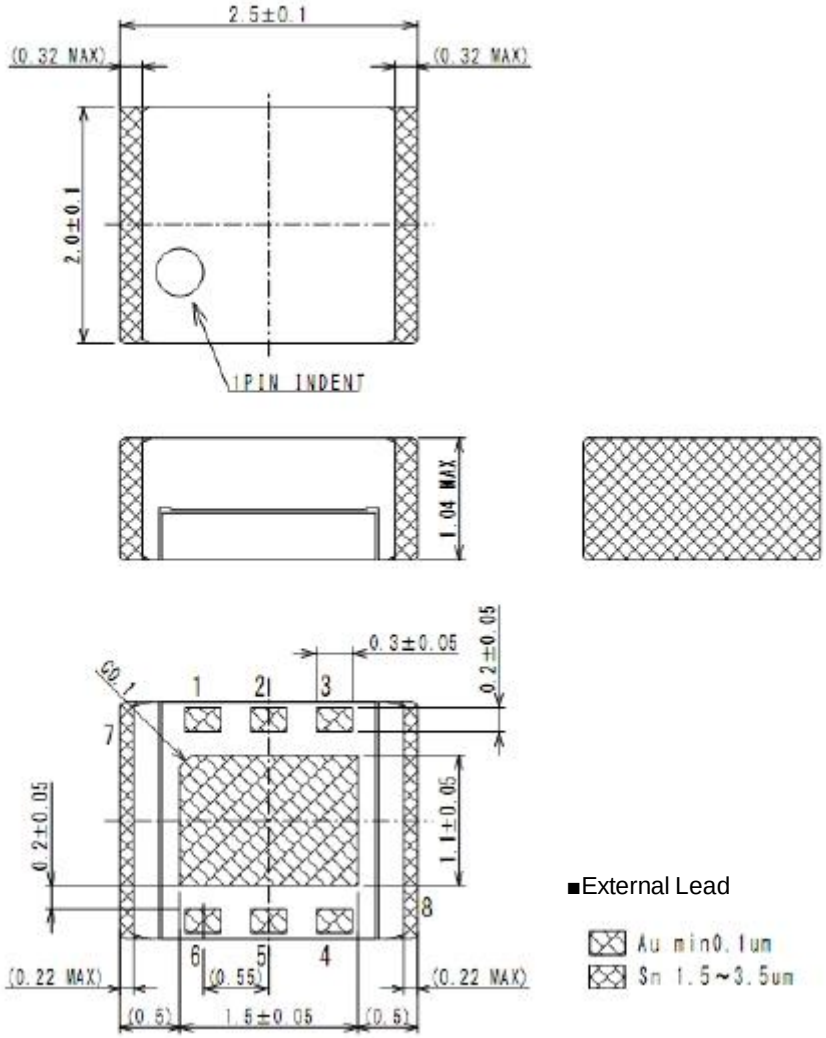


●Reference Metal Mask Design (unit:mm)



■PACKAGING INFORMATION

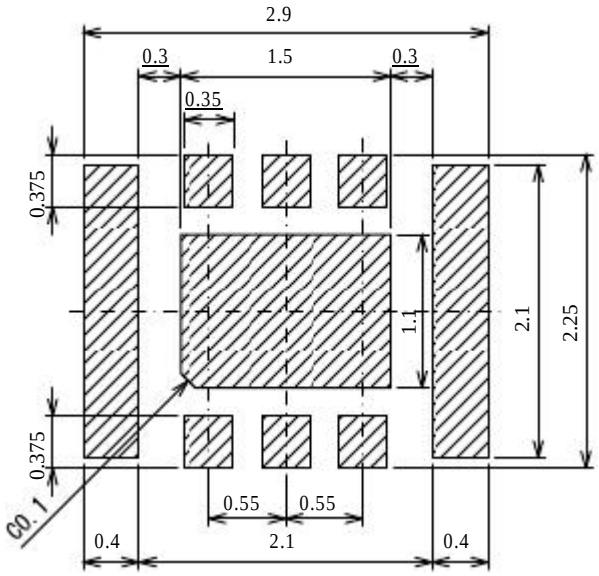
●CL-2025-02 (unit:mm)



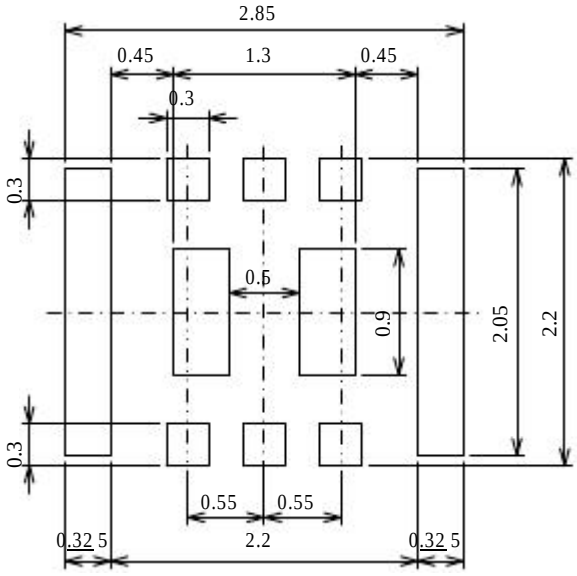
■External Lead

Au min0.1um
Sn 1.5~3.5um

●Reference Pattern Layout (unit:mm)

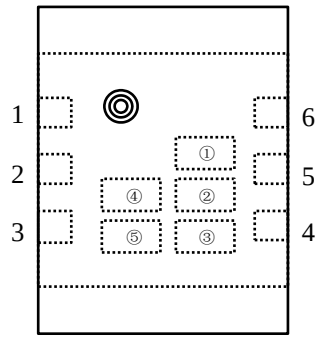


●Reference Metal Mask Design (unit:mm)



*Implementation of CL-2025-02 is recommended within accuracy 0.05mm.

■MARKING RULE



CL-2025/CL-2025-02

① represents products series

MARK	PRODUCT SERIES
F	JTMT201B*****-G
H	JTMT202B*****-G

② represents integer of output voltage and oscillation frequency

OUTPUT VOLTAGE (V)	MARK
	OSCILLATION FREQUENCY=1.2MHz (JTMT20****1**-G)
0.x	F
1.x	H
2.x	K
3.x	L
4.x	M

③ represents the decimal part of output voltage

OUTPUT VOLTAGE (V)	MARK	PRODUCT SERIES
X.0	0	JTMT20***0***-G
X.05	A	JTMT20***A***-G
X.1	1	JTMT20***1***-G
X.15	B	JTMT20***B***-G
X.2	2	JTMT20***2***-G
X.25	C	JTMT20***C***-G
X.3	3	JTMT20***3***-G
X.35	D	JTMT20***D***-G
X.4	4	JTMT20***4***-G
X.45	E	JTMT20***E***-G
X.5	5	JTMT20***5***-G
X.55	F	JTMT20***F***-G
X.6	6	JTMT20***6***-G
X.65	H	JTMT20***H***-G
X.7	7	JTMT20***7***-G
X.75	K	JTMT20***K***-G
X.8	8	JTMT20***8***-G
X.85	L	JTMT20***L***-G
X.9	9	JTMT20***9***-G
X.95	M	JTMT20***M***-G

Example (Mark ②, ③)

OSCILLATION FREQUENCY	MARK					
	JTMT20**33***-G		JTMT 20**2C***-G		JTMT 20**1L***-G	
	②	③	②	③	②	③
1.2MHz	L	3	K	C	H	L

④,⑤ represents production lot number

01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ, B1～ZZ in order.

(G, I, J, O, Q, W eJTMTuded)

*No character inversion used.

1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.

2. The information in this datasheet is intended to illustrate the operation and characteristics of our products. We neither make warranties or representations with respect to the accuracy or completeness of the information contained in this datasheet nor grant any license to any intellectual property rights of ours or any third party concerning with the information in this datasheet.

3. Applicable export control laws and regulations should be complied and the procedures required by such laws and regulations should also be followed, when the product or any information contained in this datasheet is exported.

4. The product is neither intended nor warranted for use in equipment of systems which require extremely high levels of quality and/or reliability and/or a malfunction or failure which may cause loss of human life, bodily injury, serious property damage including but not limited to devices or equipment used in 1) nuclear facilities, 2) aerospace industry, 3) medical facilities, 4) automobile industry and other transportation industry and 5) safety devices and safety equipment to control combustions and explosions. Do not use the product for the above use unless agreed by us in writing in advance.

5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.

6. Our products are not designed to be Radiation-resistant.

7. Please use the product listed in this datasheet within the specified ranges.

8. We assume no responsibility for damage or loss due to abnormal use.

9.

JIATAIMU SEMICONDUCTOR LTD.